1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB

DVT Build - 12/02/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
12		412764	ENGINEERING RELEASE	12/03/05	

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	N/A	N/A
2	2	System Block Diagram	N/A	N/A
3	3	Power Block Diagram	N/A	N/A
4	4	BOM Configuration	N/A	N/A
5	5	Functional / ICT Test	N/A	N/A
6	6	Signal Aliases	N/A	N/A
7	7	CPU 1 OF 2-FSB	M42	11/16/2005
8	8	CPU 2 OF 2-PWR/GND	M42	11/16/2005
9	9	CPU Decoupling & VID	(MASTER)	(MASTER)
10	10	CPU MISC1-TEMP SENSOR	M42	10/07/2005
11	11	CPU ITP700FLEX DEBUG	M42	10/12/2005
12	12	NB CPU Interface	(MASTER)	(MASTER)
13	13	NB PEG / Video Interfaces	(MASTER)	(MASTER)
14	14	NB Misc Interfaces	(MASTER)	(MASTER)
15	15	NB DDR2 Interfaces	(MASTER)	(MASTER)
16	16	NB Power 1	(MASTER)	(MASTER)
17	17	NB Power 2	(MASTER)	(MASTER)
18	18	NB Grounds	(MASTER)	(MASTER)
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)
20	20	NB Config Straps	(MASTER)	(MASTER)
21	21	SB: 1 OF 4	M38	11/16/2005
22	22	SB: 2 of 4	(M38)	09/08/2005
23	23	SB: 3 OF 4	M38	11/16/2005
24	24	SB: 4 OF 4	M38	11/16/2005
25	25	SB Decoupling	M42	11/16/2005
26	26	SB Misc	(MASTER)	(MASTER)
27	27	M1 SMBus Connections	(MASTER)	(MASTER)
28	28	DDR2 SO-DIMM Connector A	(MASTER)	(MASTER)
29	29	DDR2 SO-DIMM Connector B	(MASTER)	(MASTER)
30	30	Memory Active Termination	(MASTER)	(MASTER)
31	31	Memory Vtt Supply	(MASTER)	(MASTER)
32	32	DDR2 VRef	(MASTER)	(MASTER)
33	33	CLOCKS	M42	10/12/2005
34	34	Clock Termination	(MASTER)	(MASTER)
35	37	Mobile Clocking	(MASTER)	(MASTER)
36	38	PATA Connector	(MASTER)	(MASTER)
37	41	ETHERNET CONTROLLER	M42	10/12/2005
38	42	Ethernet Connector	(MASTER)	(MASTER)
39	43	Yukon Power Control	(MASTER)	(MASTER)
40	44	FIREWIRE CONTROLLER	(M42)	08/29/2005
41	45	FireWire Port Power	(MASTER)	(MASTER)
42	46	FireWire Ports	(MASTER)	(MASTER)
43	49	Internal USB Connections	(MASTER)	(MASTER)
44	52	External USB Connector	(MASTER)	(MASTER)
45	55	Left I/O Board Connector	(MASTER)	(MASTER)
46	57	PCI-E Connections	(MASTER)	(MASTER)
47	58	SMC	M38	10/07/2005
48	59	SMC Support	(MASTER)	(MASTER)
49	60	LPC+ Debug Connector	M42	07/20/2005
50	61	Thermal Sensors	(MASTER)	(MASTER)
51	62	Current & Voltage Sensing	(MASTER)	(MASTER)
52	63	SPI BOOTROM	M42	11/16/2005
53	64	ALS Support	(MASTER)	(MASTER)
54	65	Fan Connectors	(MASTER)	(MASTER)
55	66	Sudden Motion Sensor (SMS)	(MASTER)	(MASTER)
56	67	TPM	M38	11/16/2005
57	75	IMVP6 CPU VCore Regulator	(MASTER)	(MASTER)
58	76	5V / 1.5V Power Supply	(MASTER)	(MASTER)
59	77	2.5V & 1.2V Regulators	(MASTER)	(MASTER)
60	78	1.8V Supply	(MASTER)	(MASTER)
61	79	3.3V / 1.05V Power Supplies	(MASTER)	(MASTER)
62	80	3.3V G3Hot Supply & Power Control	(MASTER)	(MASTER)
63	81	Power Aliases	(MASTER)	(MASTER)
64	82	PBus-In & Battery Connectors	(MASTER)	(MASTER)
65	84	ATI M56 PCI-E	(MASTER)	(MASTER)
66	85	GPU (M56) Core Supplies	(MASTER)	(MASTER)
67	86	ATI M56 Core Power	(MASTER)	(MASTER)
68	87	ATI M56 Frame Buffer I/F	(MASTER)	(MASTER)
69	88	GPU Straps	(MASTER)	(MASTER)
70	89	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
71	90	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
72	91	ATI M56 GPIO/DVO/Misc	(MASTER)	(MASTER)
73	93	ATI M56 Video Interfaces	(MASTER)	(MASTER)
74	94	Internal Display Connectors	(MASTER)	(MASTER)
75	97	External Display Connector	(MASTER)	(MASTER)
76	98	M1 Specific Connectors	(MASTER)	(MASTER)
77	99	LVDS Interface Pull-downs	(MASTER)	(MASTER)
78	100	Revision History	N/A	N/A
79	104	M1 Net Properties	(MASTER)	(MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH	CRITICAL	
820-1881	1	PCBF,MULLET,M1	PCB	CRITICAL	PCB_THICK
920-0342	1	PCBF,MULLET_THIN,M1	PCB	CRITICAL	PCB_THIN

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Fri Dec 2 23:03:42 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941
REV. 12

System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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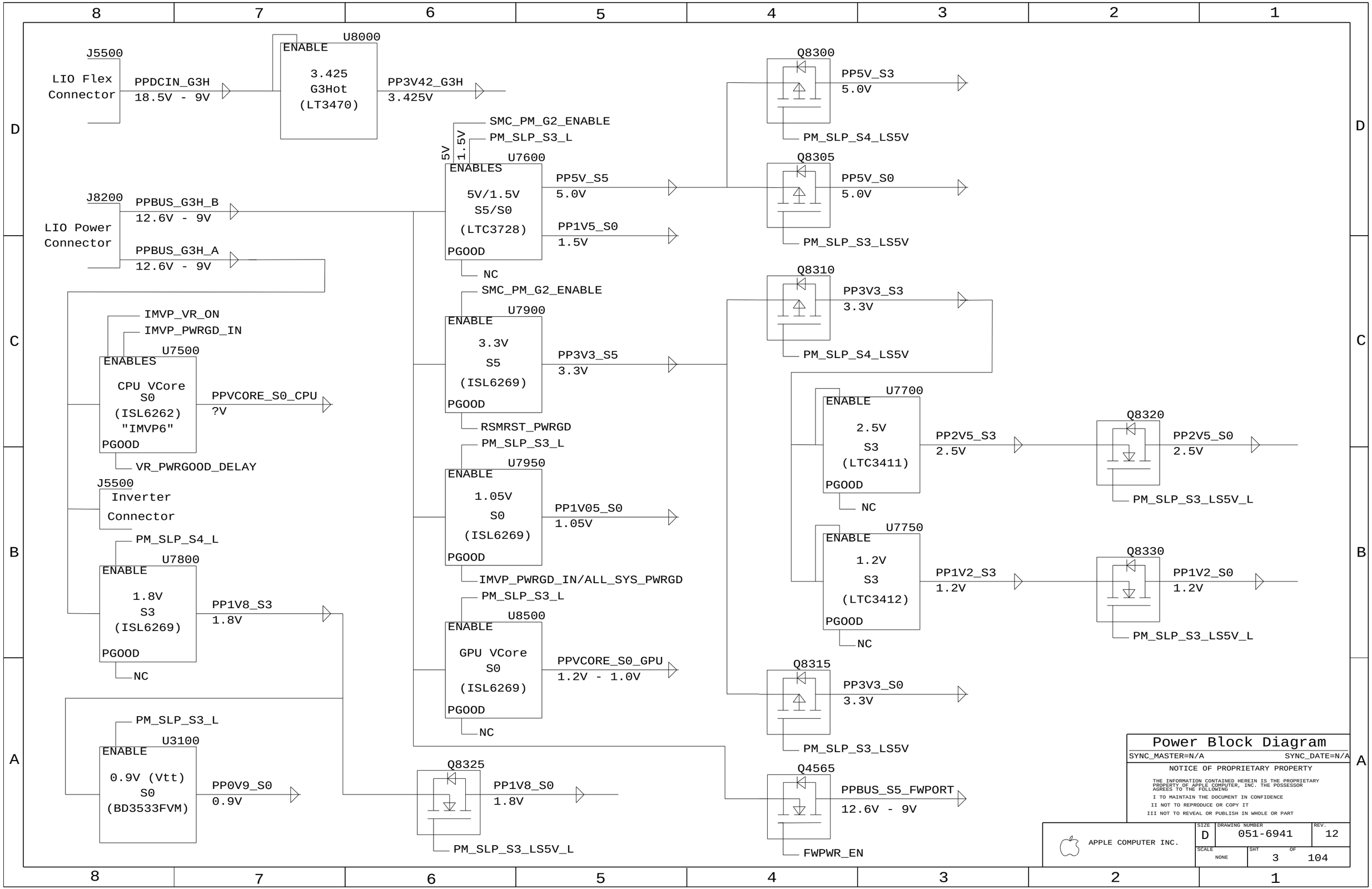
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 2 OF 104	


J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q8300
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q8305
PP5V_S0
5.0V
PM_SLP_S3_LS5V
Q8310
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
IMVP_VR_ON
IMVP_PWRGD_IN
U7500
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
?V
VR_PWRGOOD_DELAY
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
PP2V5_S3
2.5V
NC
Q8320
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
PP1V8_S3
1.8V
NC
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
NC
Q8330
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
PPVCORE_S0_GPU
1.2V - 1.0V
NC
Q8315
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q8325
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN
Power Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
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SIZE D
DRAWING NUMBER 051-6941
REV. 12
SCALE NONE
SHT 3 OF 104

"Better" BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7401	PCBA,MULLET_BTR,HY128,M1	075-0139,075-0140,075-0154,EEE_UNH
630-7403	PCBA,MULLET_BTR,SAM128,M1	075-0139,075-0140,075-0156,EEE_UNK

"Best" BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7429	PCBA,MULLET_BST,SAM128,M1	075-0139,075-0171,075-0156,EEE_UR8
630-7430	PCBA,MULLET_BST,HY128,M1	075-0139,075-0171,075-0154,EEE_UR9
630-7254	PCBA,MULLET_BST,SAM256,M1	075-0139,075-0171,075-0138,EEE_TYY
630-7402	PCBA,MULLET_BST,HY256,M1	075-0139,075-0171,075-0155,EEE_UNJ

Phantom BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
075-0139	PROJ_PTS,MULLET,M1	COMMON,M1_COMMON,M1_DEBUG,PROJ_PROTOEVTDVT
075-0140	LE_MENU,MULLET_BTR,M1	CPU_BTR,LEMENU_PROTOEVTDVT
075-0171	LE_MENU,MULLET_BST,M1	CPU_BST,LEMENU_PROTOEVTDVT
075-0156	128SAM,MULLET,M1	VRAM_128_SAMSUNG
075-0154	128HY,MULLET,M1	GPU_MEM_HYNIX,VRAM_128_HYNIX
075-0138	256SAM,MULLET,M1	GPU_MEM_256M,VRAM_256_SAMSUNG
075-0155	256HY,MULLET,M1	GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M1_COMMON	M1_COMMON1,M1_COMMON2,M1_COMMON3
M1_COMMON1	ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS,INVERTER_BUF
M1_COMMON2	KBDLED_HAS,LVDS_PD,MEMVREF_S3,MEMVTT_EN_PU,PCB_THICK
M1_COMMON3	RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU,USB_G_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0138	1	256SAM,B13,MULLET,M1	BOM3	CRITICAL	075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM1	CRITICAL	075-0139
075-0140	1	LE MENU,MULLET BTR,M1	BOM2	CRITICAL	075-0140
075-0154	1	128HY,MULLET,M1	BOM3	CRITICAL	075-0154
075-0155	1	256HY,MULLET,M1	BOM3	CRITICAL	075-0155
075-0156	1	128SAM,MULLET,M1	BOM3	CRITICAL	075-0156
075-0171	1	LE MENU,MULLET BST,M1	BOM2	CRITICAL	075-0171

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TYY]	CRITICAL	EEE_TYY	M1,BST,SAM256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNH]	CRITICAL	EEE_UNH	M1,BTR,HY128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNJ]	CRITICAL	EEE_UNJ	M1,BST,HY256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNK]	CRITICAL	EEE_UNK	M1,BTR,SAM128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UR8]	CRITICAL	EEE_UR8	M1,BST,SAM128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UR9]	CRITICAL	EEE_UR9	M1,BST,HY128

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX

"LeMenu Stage #1" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	LEMENU_STAGE1
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	LEMENU_STAGE1
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	LEMENU_STAGE1
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU_STAGE1
341S1812	1	IC,EFI,BOOTROM DEVELOPMENT,M1	U6301	CRITICAL	BOOTROM_DEVEL
341S1813	1	IC,EFI,BOOTROM FINAL,M1	U6301	CRITICAL	BOOTROM_FINAL
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	LEMENU_STAGE1
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	LEMENU_STAGE1

"LeMenu Stage #2" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	LEMENU_STAGE2

"LeMenu Stage #3" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3267	1	IC,M1 BTR,479 BGA	U0700	CRITICAL	CPU_BTR
337S3268	1	IC,M1 BST,479 BGA	U0700	CRITICAL	CPU_BST
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	LEMENU_STAGE3
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	LEMENU_STAGE3

LeMenu Stage Mappings

BOM GROUP	BOM OPTIONS
LEMENU_LOCALPROTO	BOOTROM_DEVEL,LEMENU_STAGE1,LEMENU_STAGE2,LEMENU_STAGE3
LEMENU_PROTOEVTDVT	LEMENU_STAGE2,LEMENU_STAGE3
PROJ_PROTOEVTDVT	BOOTROM_DEVEL,LEMENU_STAGE1
LEMENU_PVTRAMP	LEMENU_STAGE3
PROJ_PVTRAMP	BOOTROM_FINAL,LEMENU_STAGE1,LEMENU_STAGE2

The number of parts managed as Le Menu decreases as a project progresses.
The above stages and build settings are per 8/25 strategy statement.

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE SHT 4 OF 104

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	57
TRUE		IMVP6_COMP	57
TRUE		P5VS5_RUNSS	58 62
TRUE		P1V5S0_RUNSS	58 62
TRUE		P2V5S3_MODE	59
TRUE		P2V5S3_SHDNRT	59
TRUE		P1V2S3_RT	59
TRUE		P1V2S3_RUNSS	39 59
TRUE		P1V8S3_COMP	60
TRUE		P1V8S3_FSET	60
TRUE		P3V3S5_COMP	61
TRUE		P3V3S5_FSET	61
TRUE		P1V05S0_COMP	61
TRUE		P1V05S0_FSET	61
TRUE		P3V42G3H_FB	62
TRUE		GPUVCORE_COMP	66
TRUE		GPUVCORE_FSET	66
TRUE		GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 79
TRUE		FSB_ADS_L	7 12 79
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 79
TRUE		FSB_BNR_L	7 12 79
TRUE		FSB_BREQ0_L	7 12 79
TRUE		FSB_D_L<63..0>	7 12 79
TRUE		FSB_DBSY_L	7 12 79
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 79
TRUE		FSB_DRDY_L	7 12 79
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 79
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 79
TRUE		FSB_HIT_L	7 12 79
TRUE		FSB_HITM_L	7 12 79
TRUE		FSB_LOCK_L	7 12 79
TRUE		FSB_REQ_L<4..0>	7 12 79

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST		
	=PP5V_S0_FAN_LT	54 63
	FAN_LT_PWM	54
	FAN_LT_TACH	54
	FAN_RT_PWM	54
	FAN_RT_TACH	54

LPC+ Debug Connector

FUNC_TEST		
TRUE	=PP3V3_S5_LPCPLUS	49 63
TRUE	=PP5V_S0_LPCPLUS	49 63
TRUE	LPC_AD<0>	21 47 49 56
TRUE	LPC_AD<1>	21 47 49 56
TRUE	LPC_FRAME_L	21 47 49 56
TRUE	PM_CLKRUN_L	23 40 47 49 56
TRUE	BOOT_LPC_SPI_L	22 47 49
TRUE	SMC_TMS	47 48 49
TRUE	DEBUG_RST_L	26 49
TRUE	SMC_TRST_L	47 49
TRUE	SMC_TDO	47 48 49
TRUE	SMC_MD1	47 49
TRUE	SMC_TX_L	47 48 49
TRUE	FWH_INIT_L	21 48 49
TRUE	PCI_CLK_PORT80_LPC	34 49
TRUE	LPC_AD<2>	21 47 49 56
TRUE	LPC_AD<3>	21 47 49 56
TRUE	INT_SERIRQ	23 47 49 56
TRUE	PM_SUS_STAT_L	23 47 48 49 56
TRUE	SMC_TDI	47 48 49
TRUE	SMC_TCK	47 48 49
TRUE	SMC_RST_L	47 48 49
TRUE	SMC_NMI	47 49
TRUE	SMC_RX_L	47 48 49
TRUE	SV_SET_UP	23 49

Left ALS Connector

FUNC_TEST		
TRUE	=PP3V3_S3_LTALS	63 76
TRUE	ALS_GAIN	6 47 76
TRUE	LTALS_OUT	53 76
TRUE	GND\g	

Camera Connector

FUNC_TEST		
TRUE	=PP5V_S3_CAMERA	43 63
TRUE	=USB2_CAMERA_N	6 43
TRUE	=USB2_CAMERA_P	6 43
TRUE	=SMBUS_ATS_SDA	27 43
TRUE	=SMBUS_ATS_SCL	27 43
TRUE	GND\g	

Thermal Diode Connectors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	50
TRUE	HSTHMSNS_DX_N	50
TRUE	RSFSTHMSNS_D_P	50
TRUE	RSFSTHMSNS_D_N	50

Other Func Test Points

FUNC_TEST		
TRUE	=PP1V05_S0_REG	51 61 63
TRUE	PM_SYSRST_L	23 26 47
TRUE	SMC_ONOFF_L	43 47 48 51

Current Sense Calibration

FUNC_TEST		
TRUE	ISENSE_CAL_EN	
TRUE	=PP5V_S0_ISENSECAL	
TRUE	PP1V8_S3_REG	63
TRUE	PP1V5_S0_REG	63
TRUE	PPVCORE_S0_GPU	63
TRUE	PPVCORE_S0_CPU	63
TRUE	GND\g	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST		
TRUE	SMC_BS_ALRT_L	47 48 64
TRUE	=SMBUS_BATT_SCL	27 64
TRUE	=SMBUS_BATT_SDA	27 64
TRUE	GND_BATT	64

Left I/O Data Connector

FUNC_TEST		
TRUE	=PP1V5_S0_LIO	45 63
TRUE	=PPDCIN_G3H_LIO	45 63
TRUE	=PP5V_S5_LIO	45 63
TRUE	=PP3V42_G3H_LIO	45 63
TRUE	PP5V_S0_AUDIO_PWR	45
TRUE	PP5V_S0_AUDIO	45
TRUE	GND_AUDIO_PWR	45
TRUE	GND_AUDIO	45
TRUE	ACZ_SDATAIN<0>	21 45 79
TRUE	ACZ_SDATAOUT	21 45 79
TRUE	ACZ_BITCLK	21 45 79
TRUE	ACZ_RST_L	21 45 79
TRUE	EXCARD_OC_L	6 45 48
TRUE	LTUSB_OC_L	6 45
TRUE	LIO_BATT_ISENSE	45 51
TRUE	SMC_SYS_ISET	45 47
TRUE	SMC_BATT_ISET	45 47
TRUE	SMC_BATT_CHG_EN	45 47 48
TRUE	SMC_BC_ACOK	45 47 48
TRUE	SMC_ADAPTER_EN	41 45 47 48
TRUE	LIO_P3V3S0_EN_L	45 62
TRUE	LIO_DCIN_ISENSE	45 51
TRUE	LIO_P3V3S3_EN	45 62
TRUE	SMC_BATT_TRICKLE_EN_L	45 47 48
TRUE	SYS_ONEWIRE	45 47 48
TRUE	MINI_CLKREQ_L	34 45
TRUE	SMC_EXCARD_CP	45 47 48
TRUE	EXCARD_CLKREQ_L	34 45
TRUE	SMC_EXCARD_PWR_EN	45 47
TRUE	LIO_PLT_RESET_L	26 45
TRUE	ACZ_SYNC	21 45 79
TRUE	=USB2_LT_N	6 45
TRUE	=USB2_LT_P	6 45
TRUE	=USB2_EXCARD_N	6 45
TRUE	=USB2_EXCARD_P	6 45
TRUE	=PCIE_EXCARD_R2D_N	45 46
TRUE	=PCIE_EXCARD_R2D_P	45 46
TRUE	=PCIE_EXCARD_D2R_N	45 46
TRUE	=PCIE_EXCARD_D2R_P	45 46
TRUE	PCIE_CLK100M_EXCARD_P	34 45
TRUE	PCIE_CLK100M_EXCARD_N	34 45
TRUE	=PCIE_MINI_R2D_N	45 46
TRUE	=PCIE_MINI_R2D_P	45 46
TRUE	=PCIE_MINI_D2R_N	45 46
TRUE	=PCIE_MINI_D2R_P	45 46
TRUE	PCIE_CLK100M_MINI_P	34 45
TRUE	PCIE_CLK100M_MINI_N	34 45
TRUE	=SMBUS_LIO_SMC_SCL	27 45
TRUE	=SMBUS_LIO_SMC_SDA	27 45
TRUE	=SMBUS_LIO_SB_SCL	27 45
TRUE	=SMBUS_LIO_SB_SDA	27 45
TRUE	PCIE_WAKE_L	23 37 45

Left I/O Power Connector

FUNC_TEST		
TRUE	=PPBUS_G3H_LIO_CONN	63 64
TRUE	GND\g	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

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NC_CPU_A32_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A32_L (7)
NC_CPU_A33_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A33_L (7)
NC_CPU_A34_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A34_L (7)
NC_CPU_A35_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A35_L (7)
NC_CPU_A36_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A36_L (7)
NC_CPU_A37_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A37_L (7)
NC_CPU_A38_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A38_L (7)
NC_CPU_A39_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_A39_L (7)
NC_CPU_APM0_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_APM0_L (7)
NC_CPU_APM1_L (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_APM1_L (7)
NC_CPU_EXTBREF (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_EXTBREF (7)
NC_CPU_HFPLL (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_HFPLL (7)
NC_CPU_SPARE0 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_SPARE0 (7)
NC_CPU_SPARE1 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_SPARE1 (7)
NC_CPU_SPARE2 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_SPARE2 (7)
NC_CPU_SPARE4 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_CPU_SPARE4 (7)

NC_MEM_A_A<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	MEM_A_A<15..14> (28)
NC_MEM_B_A<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	MEM_B_A<15..14> (29)
TP_NB_CFG<4..3> (MAKE_BASE=TRUE)	—	NB_CFG<4..3> (14)
TP_NB_CFG<6> (MAKE_BASE=TRUE)	—	NB_CFG<6> (14)
TP_NB_CFG<8> (MAKE_BASE=TRUE)	—	NB_CFG<8> (14)
TP_NB_CFG<11..10> (MAKE_BASE=TRUE)	—	NB_CFG<11..10> (14)
TP_NB_CFG<15..14> (MAKE_BASE=TRUE)	—	NB_CFG<15..14> (14)
TP_NB_CFG<17> (MAKE_BASE=TRUE)	—	NB_CFG<17> (14)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> (MAKE_BASE=TRUE)	—	NB_CFG<13..12> (14)
TP_SB_SUS_CLK (MAKE_BASE=TRUE)	—	SUS_CLK_SB (23)
NC_SB_XOR_T5 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_SB_XOR_T5 (21)
NC_SB_XOR_U5 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_SB_XOR_U5 (21)
NC_SB_XOR_V3 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_SB_XOR_V3 (21)
NC_SB_XOR_V4 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_SB_XOR_V4 (21)
NC_SB_XOR_W3 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	TP_SB_XOR_W3 (21)

TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)	—	SMC_RSTGATE_L (47)
(76 47 5) ALS_GAIN (MAKE_BASE=TRUE)	—	=RTALS_GAIN (53)
NC_ENET_CTRL12 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	ENET_CTRL12 (37)
NC_ENET_CTRL25 (MAKE_BASE=TRUE, NO_TEST=TRUE)	—	ENET_CTRL25 (37)

Ethernet Power Management Support

ENET_LOM_DISABLE

R0600 0 5% 1/16W MF-LF 402

(22) IN SB_GPIO30 — 1 — 2 — ENET_LOM_DIS_L OUT (37)

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

(44) =USB2_RT_P	—	USB2_RT_P (MAKE_BASE=TRUE)	—	USB_A_P (22)
(44) =USB2_RT_N	—	USB2_RT_N (MAKE_BASE=TRUE)	—	USB_A_N (22)
(44) =RTUSB_OC_L	—	RTUSB_OC_L (MAKE_BASE=TRUE)	—	USB_A_OC_L (22)

USB Port "B" = Trackpad (Geyser)

(43) =USB_TRACKPAD_P	—	USB_TRACKPAD_P (MAKE_BASE=TRUE)	—	USB_B_P (22)
(43) =USB_TRACKPAD_N	—	USB_TRACKPAD_N (MAKE_BASE=TRUE)	—	USB_B_N (22)
UNUSED_USB_B_OC_L (MAKE_BASE=TRUE)			—	USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

(45 5) =USB2_LT_P	—	USB2_LT_P (MAKE_BASE=TRUE)	—	USB_C_P (22)
(45 5) =USB2_LT_N	—	USB2_LT_N (MAKE_BASE=TRUE)	—	USB_C_N (22)
(45 5) LTUSB_OC_L (MAKE_BASE=TRUE)			—	USB_C_OC_L (22)

USB Port "D" = Camera

(43 5) =USB2_CAMERA_P	—	USB2_CAMERA_P (MAKE_BASE=TRUE)	—	USB_D_P (22)
(43 5) =USB2_CAMERA_N	—	USB2_CAMERA_N (MAKE_BASE=TRUE)	—	USB_D_N (22)
UNUSED_USB_D_OC_L (MAKE_BASE=TRUE)			—	USB_D_OC_L (22)

USB Port "E" = ExpressCard

(45 5) =USB2_EXCARD_P	—	USB2_EXCARD_P (MAKE_BASE=TRUE)	—	USB_E_P (22)
(45 5) =USB2_EXCARD_N	—	USB2_EXCARD_N (MAKE_BASE=TRUE)	—	USB_E_N (22)
(48 45 5) EXCARD_OC_L (MAKE_BASE=TRUE)			—	USB_E_OC_L (22)

USB Port "F" = IR Receiver

(76) =USB_IR_P	—	USB_IR_P (MAKE_BASE=TRUE)	—	USB_F_P (22)
(76) =USB_IR_N	—	USB_IR_N (MAKE_BASE=TRUE)	—	USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

(76) =USB_BT_P	—	USB_BT_P (MAKE_BASE=TRUE)	—	USB_G_P (22)
(76) =USB_BT_N	—	USB_BT_N (MAKE_BASE=TRUE)	—	USB_G_N (22)

USB Port "H" = Reserved (PCI-E Mini Card)

		TP_USB2_HP (MAKE_BASE=TRUE)	—	USB_H_P (22)
		TP_USB2_HN (MAKE_BASE=TRUE)	—	USB_H_N (22)

Trace deleted to make room for other diffpairs over RAM connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600 HOLE-VIA-P5RP25 — 1 — GND_CHASSIS_DVI_TOP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

	—	=GND_CHASSIS_DVI2 (75)
	—	=GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601 HOLE-VIA-P5RP25 — 1 — GND_CHASSIS_DVI_BOT (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

	—	=GND_CHASSIS_DVI1 (75)
	—	=GND_CHASSIS_DVI3 (75)
	—	=GND_CHASSIS_DVI5 (75)
	—	=GND_CHASSIS_ENET (38)
	—	=GND_CHASSIS_FW_EMI (42)
	—	=GND_CHASSIS_FW_PORT1 (42)
	—	=GND_CHASSIS_RTUSB (44)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25 — 1 — GND_CHASSIS_LVDS (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

	—	=GND_CHASSIS_LCD1 (74)
	—	=GND_CHASSIS_LCD2 (74)
	—	=GND_CHASSIS_LCD3 (74)
	—	=GND_CHASSIS_LCD4 (74)

SH0600 OG-503040 SHLD-SM-LF — 1, 2, 3 — GND_CHASSIS_INVERTER (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)

	—	=GND_CHASSIS_INVERTER (74)

Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

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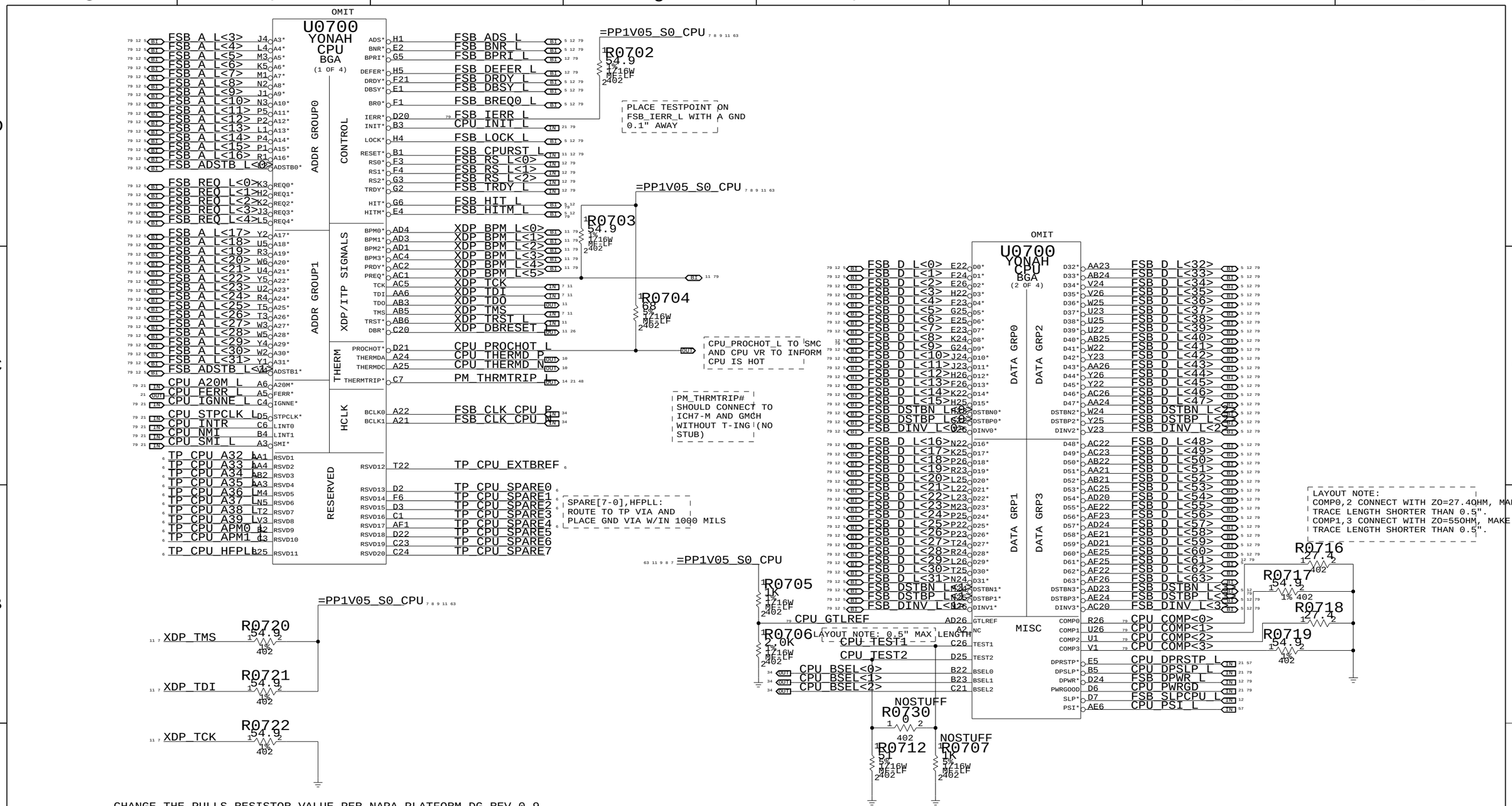

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

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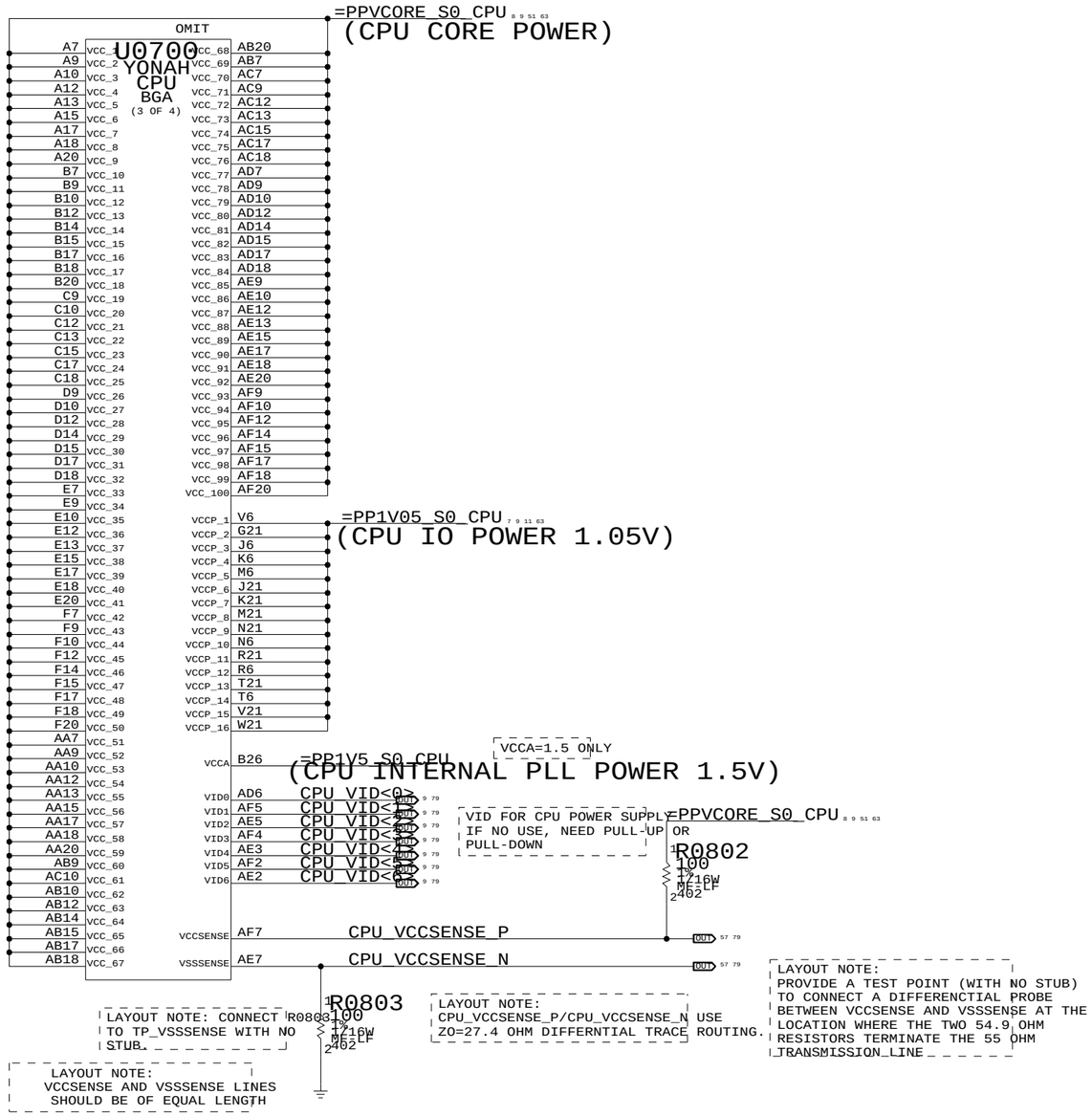

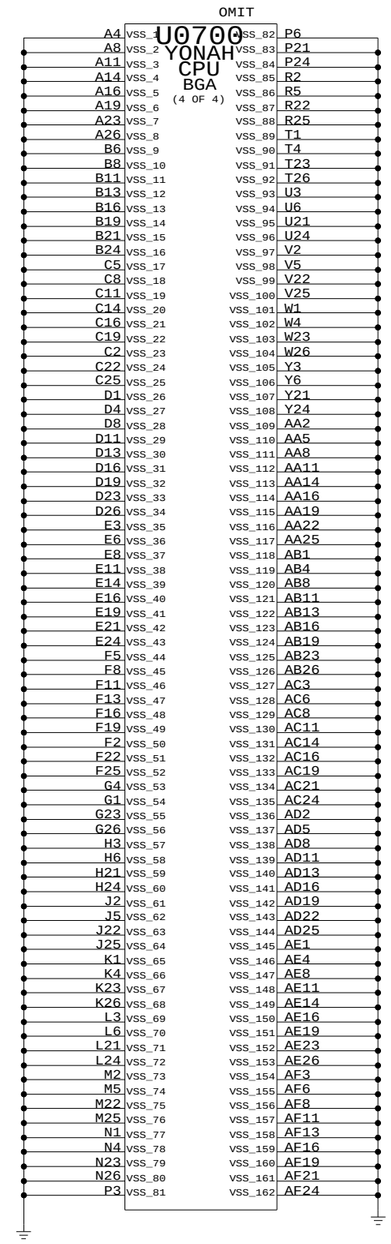

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

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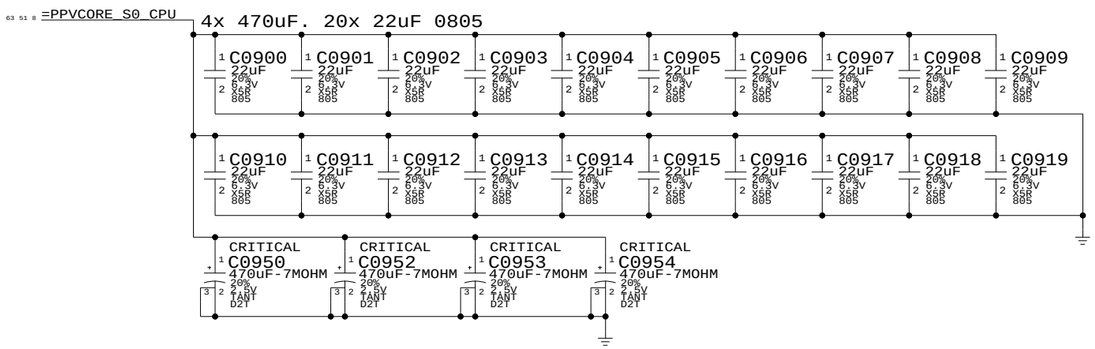
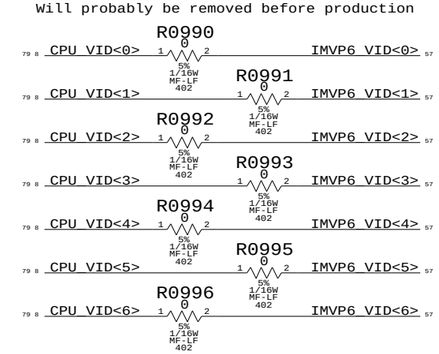
CPU VCORE HF AND BULK DECOUPLING

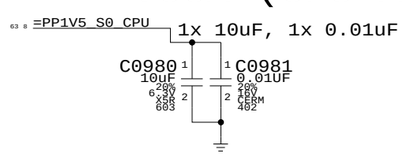


CPU VCORE VID Connections

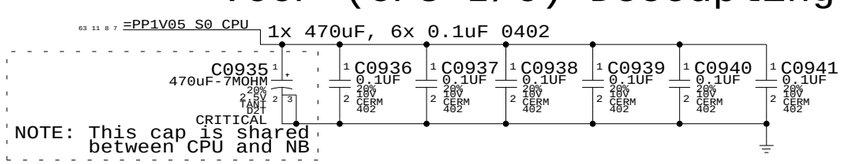
Resistors to allow for override of CPU VID
Will probably be removed before production



VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling



CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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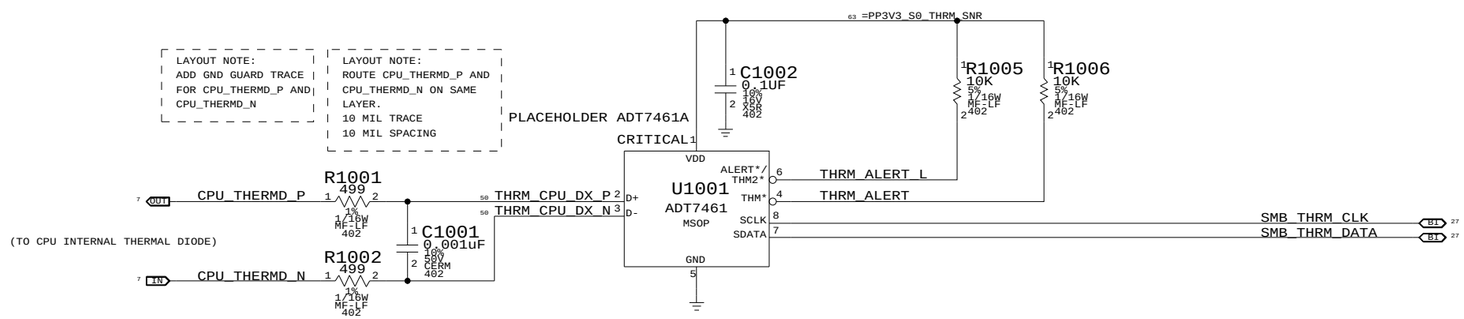
CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42 SYNC_DATE=10/07/2005

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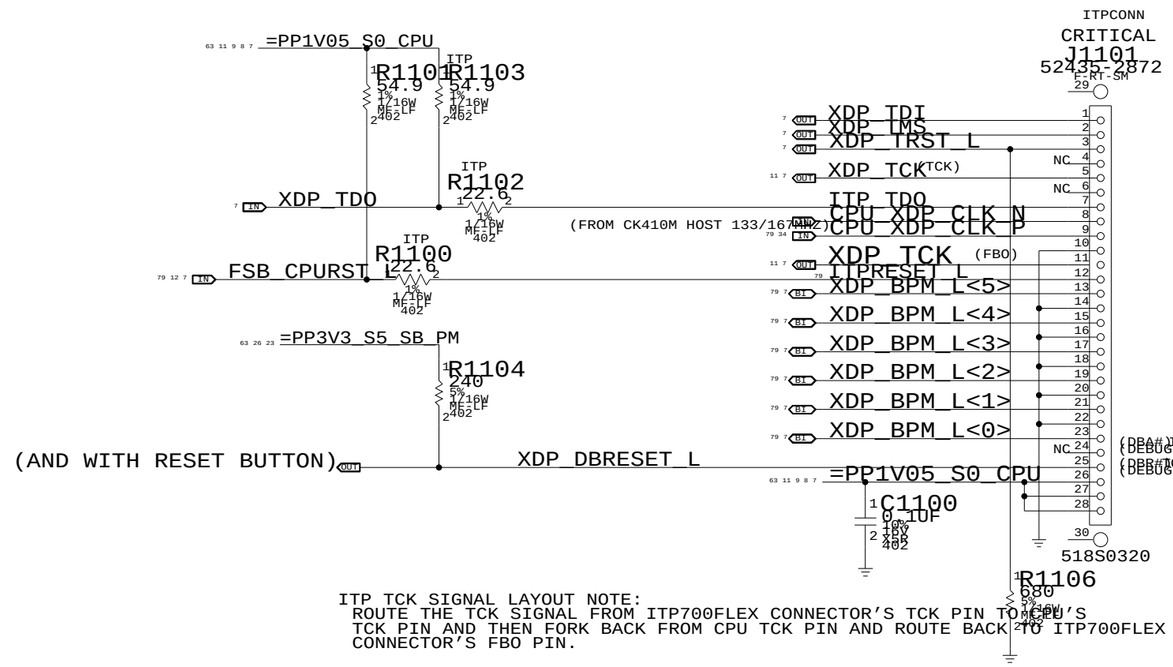
CPU ITP700FLEX DEBUG SUPPORT



(DBA# INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBRESET TCH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MAX SYNC_DATE=10/12/2005

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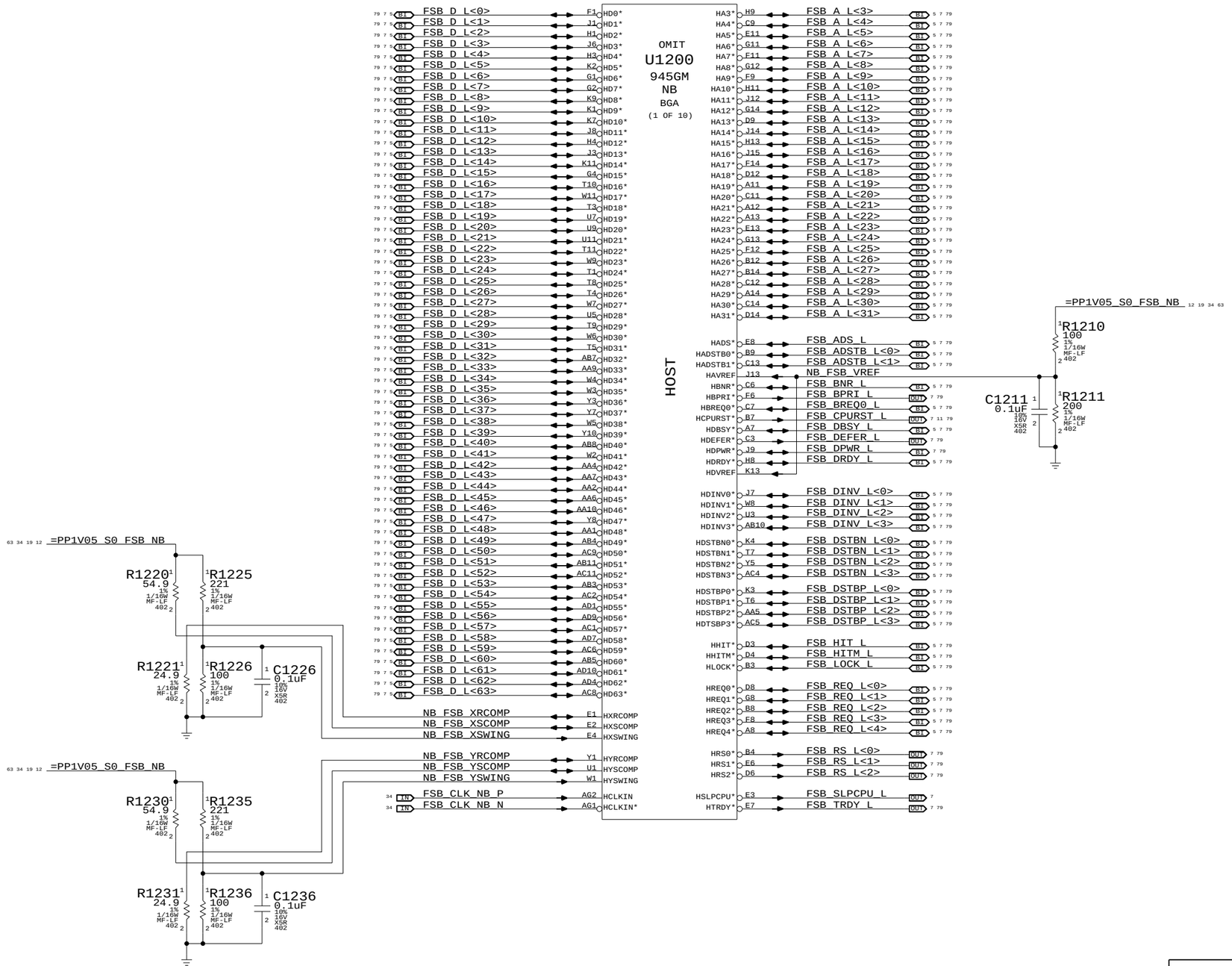

NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

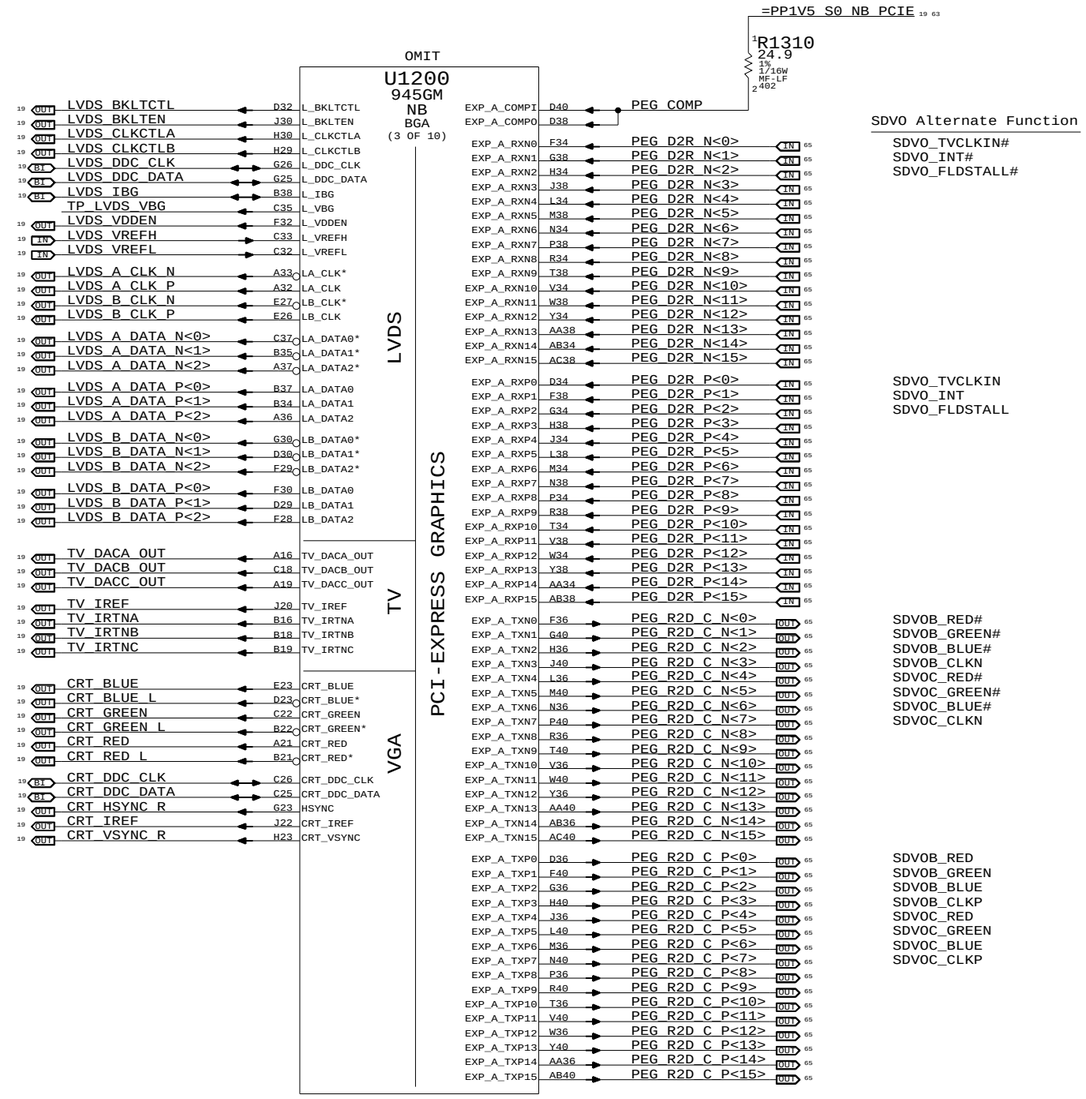
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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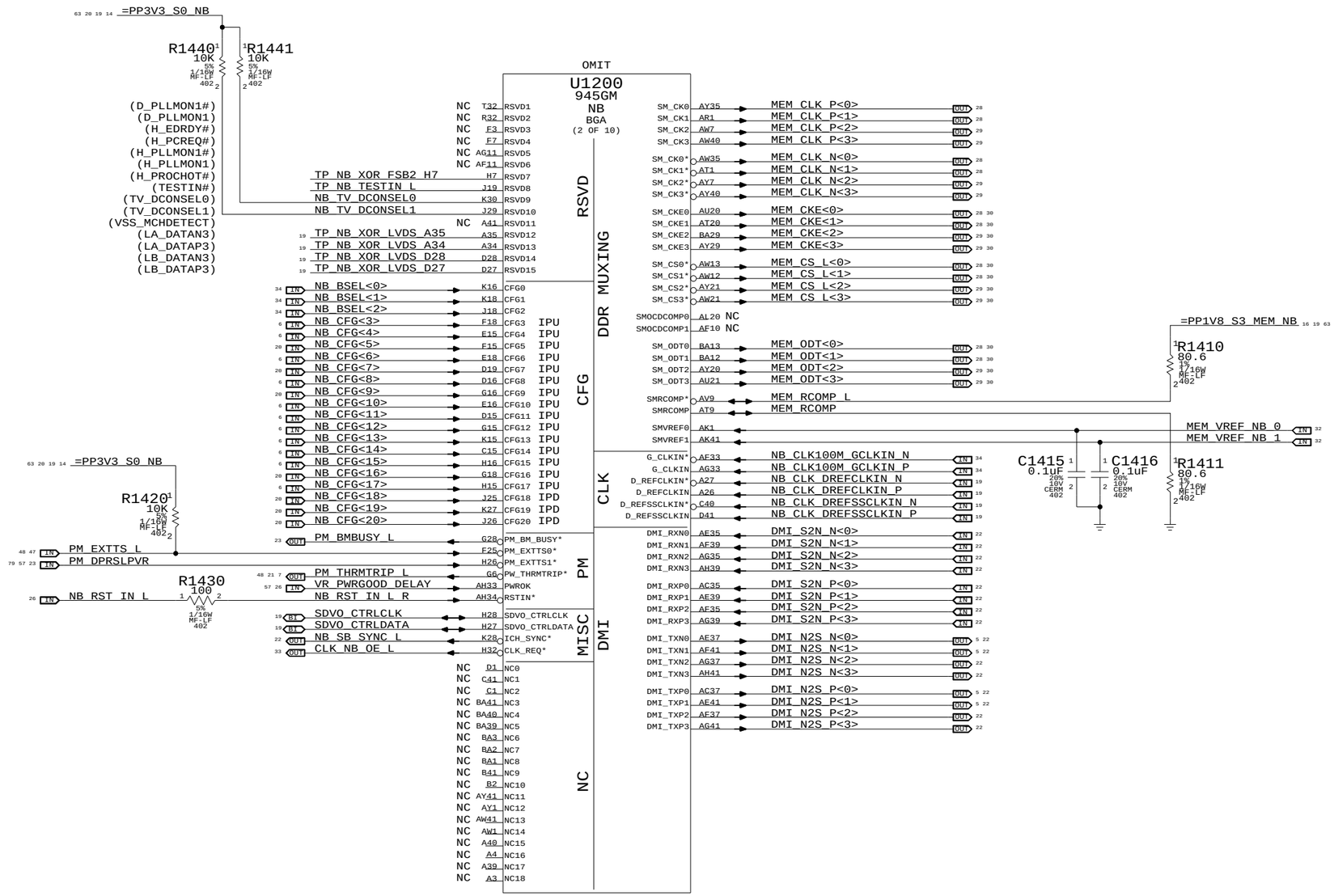

NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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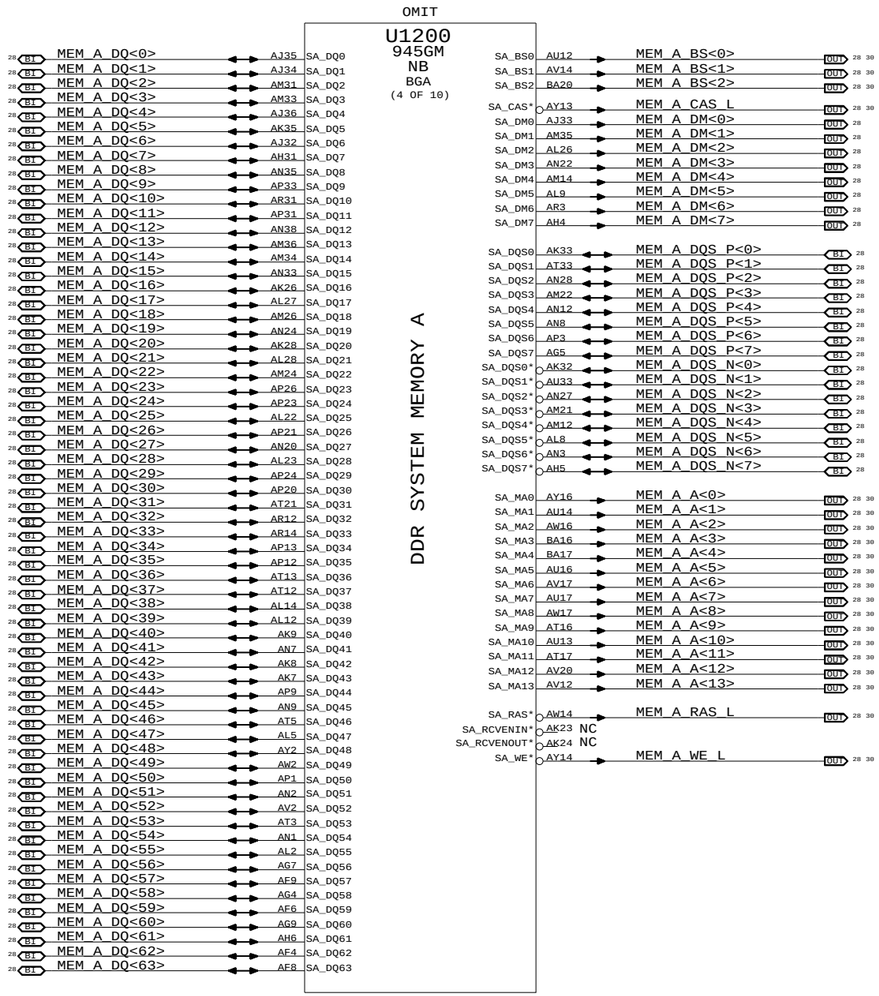

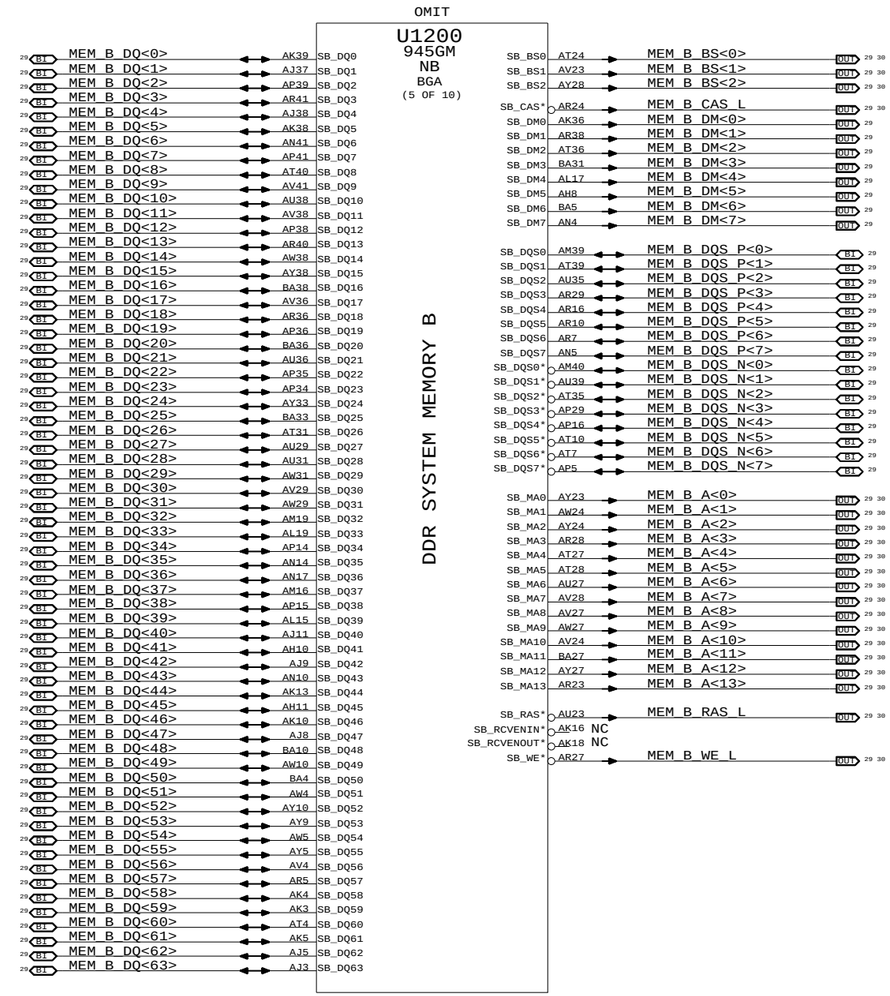

NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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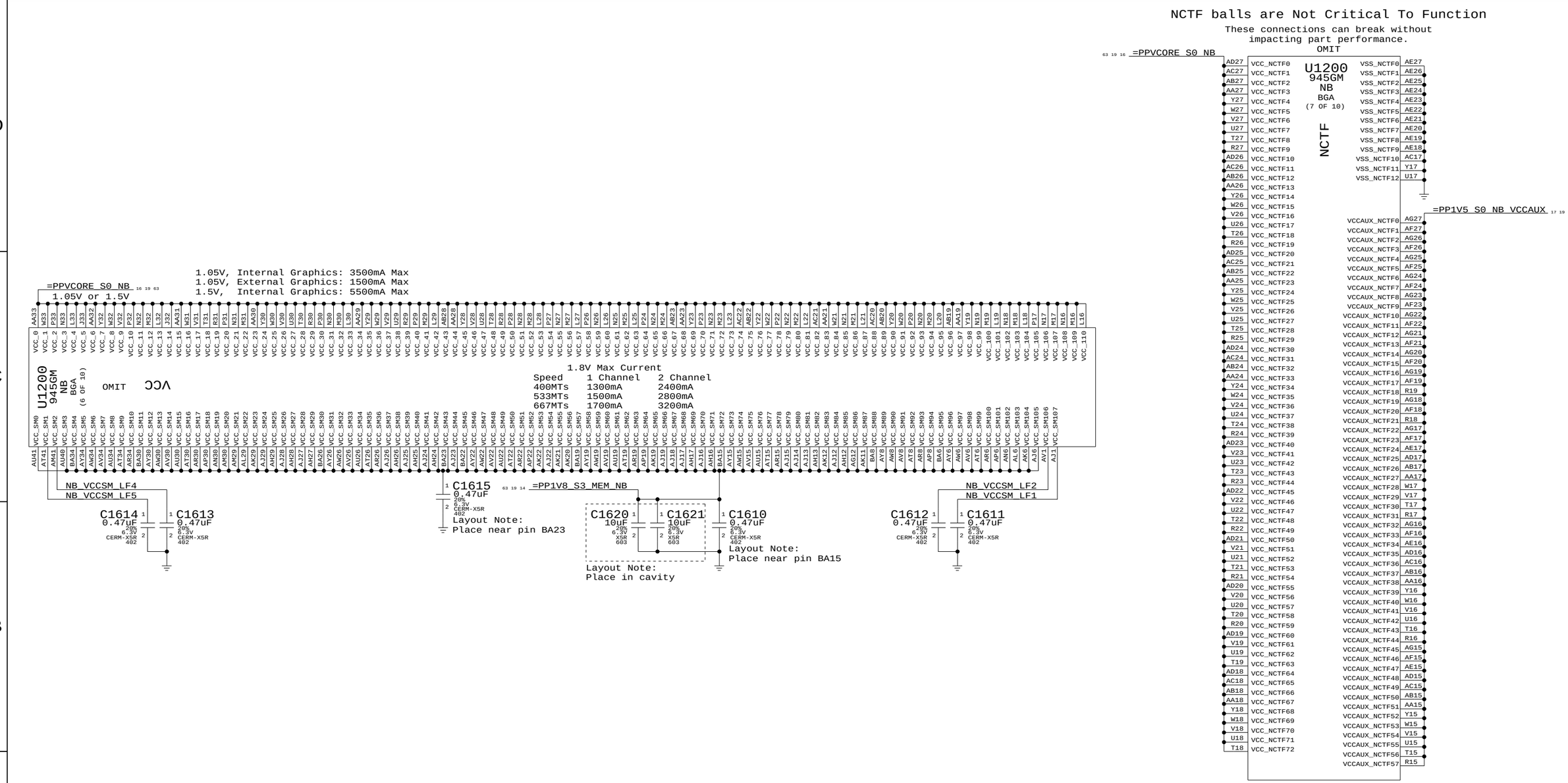

NB Power 1

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SCALE NONE

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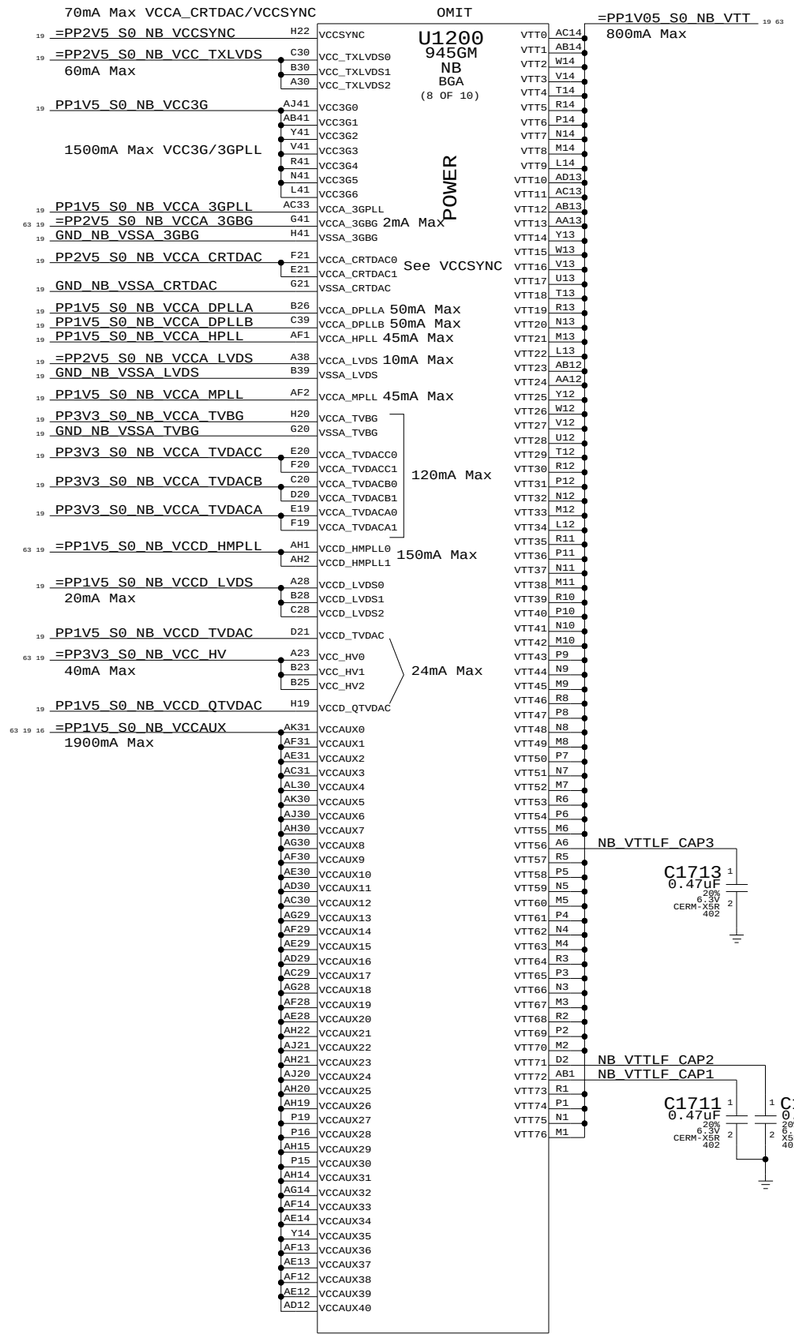

NB Power 2

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OMIT

U1200
945GM
NB
BGA
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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12

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NONE	18	104

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	1500mA Max
	=PP1V05_S0_FSB_NB	10mA Max?
	=PP1V05_S0_NB_VTT	800mA Max
	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	=PP1V5_S0_NB	?mA Max
	=PP1V5_S0_NB_3G	>1500mA Max
	=PP1V5_S0_NB_3GPLL	
	=PP1V5_S0_NB_PCIE	?mA Max
	=PP1V5_S0_NB_PLL	100mA Max
	=PP1V5_S0_NB_TVDAC	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	3200mA Max
132mA Max	=PP2V5_S0_NB_VCCSYNC	70mA Max
	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
40mA Max?	=PP3V3_S0_NB	?mA Max
	=PP3V3_S0_NB_VCC_HV	40mA Max

63 19 =PP1V05_S0_NB_CRT
- CRT_RED 13
- CRT_GREEN 13
- CRT_BLUE 13
- CRT_RED_L 13
- CRT_GREEN_L 13
- CRT_BLUE_L 13
- CRT_IREF 13
- CRT_HSYNC_R 13
- CRT_VSYNC_R 13

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK 13

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA 13

63 19 =PP1V5_S0_NB_TVDAC
- TV_DACA_OUT 13
- TV_DACB_OUT 13
- TV_DACC_OUT 13
- TV_IREF 13
- TV_IRTNA 13
- TV_IRTNB 13
- TV_IRTNC 13

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL 13

TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN 13

TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA 13

TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB 13

TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK 13

TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA 13

NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG 13

TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN 13

NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH 13

TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL 13

NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P 13

NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N 13

NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> 13

NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> 13

NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P 13

NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N 13

NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> 13

NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> 13

NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 14

NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 14

NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 14

NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 14

TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK 14

TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA 14

(MCH LVDS DATA/CLK TX 2.5V PWR)
=PP2V5_S0_NB_VCC_TXLVDS 17 19

(MCH LVDS DIGITAL 1.5V PWR)
=PP1V5_S0_NB_VCCD_LVDS 17

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS 17

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS 17

63 19 16 =PPVCORE_S0_NB
- (MCH CRTDAC ANALOG 2.5V PWR) PP2V5_S0_NB_VCCA_CRTDAC 17
- GND_NB_VSSA_CRTDAC 17
- (MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC 17 19

63 19 =PP1V5_S0_NB_TVDAC
- (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB_VCCD_TVDAC 17
- (MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB_VCCD_QTVDAC 17
- (MCH TV OUT CHANNEL A 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACA 17
- (MCH TV OUT CHANNEL B 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACB 17
- (MCH TV OUT CHANNEL C 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACC 17
- (MCH TV DAC BAND GAP 3.3V PWR) PP3V3_S0_NB_VCCA_TVBG 17
- GND_NB_VSSA_TVBG 17

TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — (MCH DISPLAY A PLL 1.5V PWR) PP1V5_S0_NB_VCCA_DPLLA 17

TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — (MCH DISPLAY B PLL 1.5V PWR) PP1V5_S0_NB_VCCA_DPLLB 17

- NB_CLK_DREFCLKIN_P 14
- NB_CLK_DREFCLKIN_N 14
- NB_CLK_DREFSSCLKIN_P 14
- NB_CLK_DREFSSCLKIN_N 14

63 19 16 =PPVCORE_S0_NB
1500mA Max

GMCH CORE PWR 1.05V BYPASS

CRITICAL	C1900	470uF-7MOHM	20%	2.5V	TANT	D2T	C1902	10uF	20%	6.3V	X5R	603	C1903	10uF	20%	6.3V	X5R	603	C1904	1uF	10%	6.3V	CERM	402	C1905	0.22uF	20%	6.3V	X5R	402	C1906	0.22uF	20%	6.3V	X5R	402	C1907	0.22uF	20%	6.3V	X5R	402

63 19 17 =PP1V05_S0_NB_VTT
800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)

C1965 4.7uF 20% 6.3V CERM 603 — C1966 2.2uF 20% 6.3V CERM1 603

Layout Note:
Place in cavity

(SHARE C0940 470UF)

C1967 0.22uF 20% 6.3V X5R 402

Layout Note:
Place on the edge

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

63 19 17 =PP3V3_S0_NB_VCC_HV
40mA Max

C1914 10uF 20% 6.3V X5R 603 — C1915 0.1uF 20% 10V CERM 402

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

63 19 17 =PP2V5_S0_NB_VCCA_3GBG
2mA Max

C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

63 19 17 16 =PP1V5_S0_NB_VCCAUX
1900mA Max

C1918 0.1uF 20% 10V CERM 402

63 19 =PP1V5_S0_NB_PLL
100mA Max

L1934 FERR-120-OHM-0.2A 0603

C1934 22uF 20% 6.3V X5R 805 — C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL 17
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

L1936 FERR-120-OHM-0.2A 0603

C1936 22uF 20% 6.3V X5R 805 — C1937 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL 17
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

1500mA Max

63 19 =PP1V5_S0_NB_3G

L1970 91nH 1210

C1970 220UF 20% 2.5V POS SMB2

Layout Note:
Place L and C
close to MCH

C1971 10uF 20% 6.3V X5R 603 — C1972 10uF 20% 6.3V X5R 603

Layout Note:
10uF caps should
be close to MCH
on opposite side.

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G 17
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

1500mA Max

63 19 =PP1V5_S0_NB_3GPLL

L1975 1.0UH-220MA-0.12-OHM 0805

PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V

R1975 0.51 1% 1/16W MF-LF 402

C1975 10uF 20% 6.3V X5R 603 — C1976 0.1uF 20% 10V CERM 402

Layout Note:
3GPLL 10uF cap should
be placed in cavity

GND_NB_VSSA_3GBG 17

Layout Note: Route to caps, then GND

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL 17
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 19 OF 104	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 63
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 63
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

=PP3V3_S0_NB 14 19 20 63
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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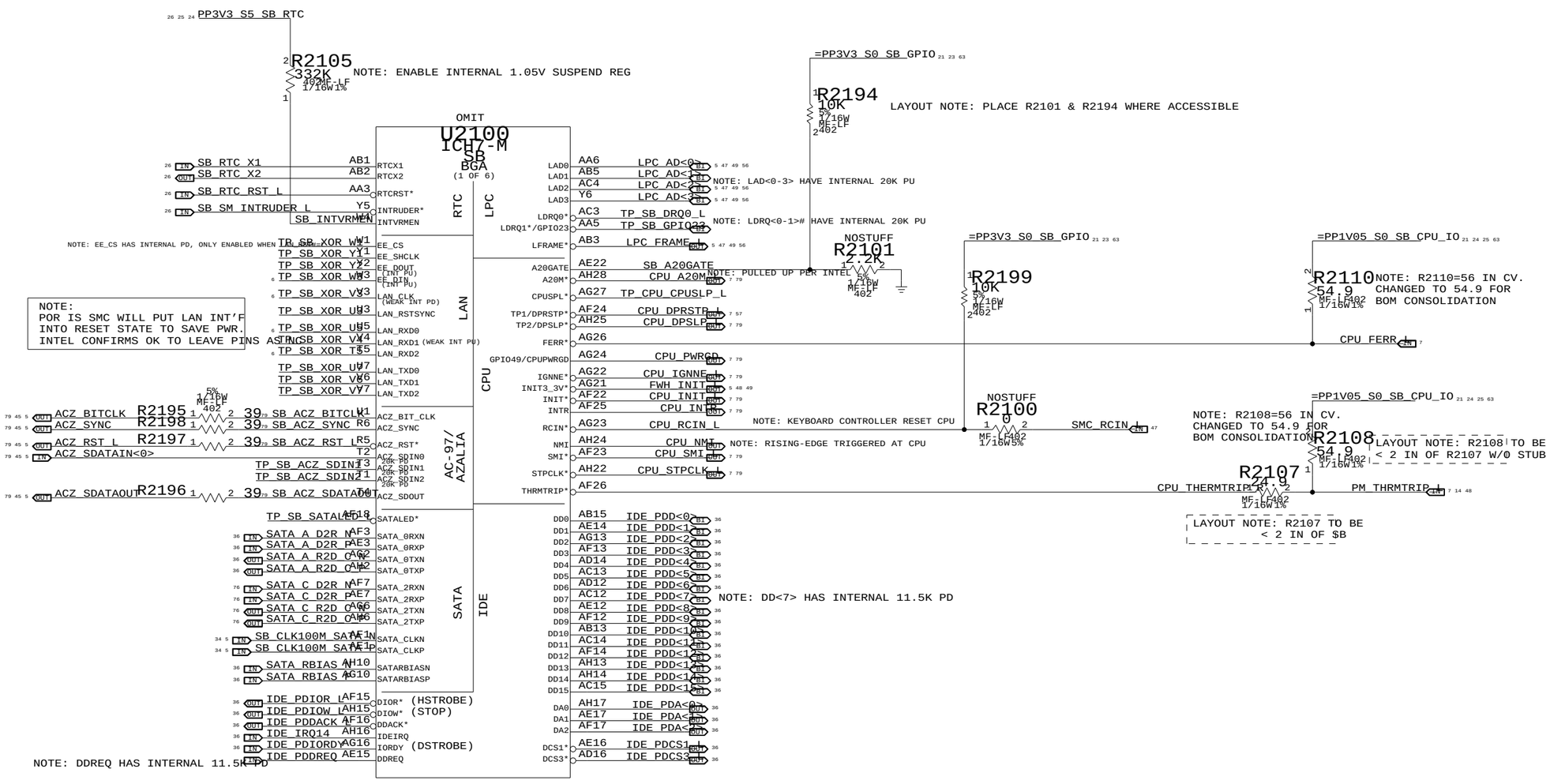
SCALE NONE SHT 20 OF 104



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE	
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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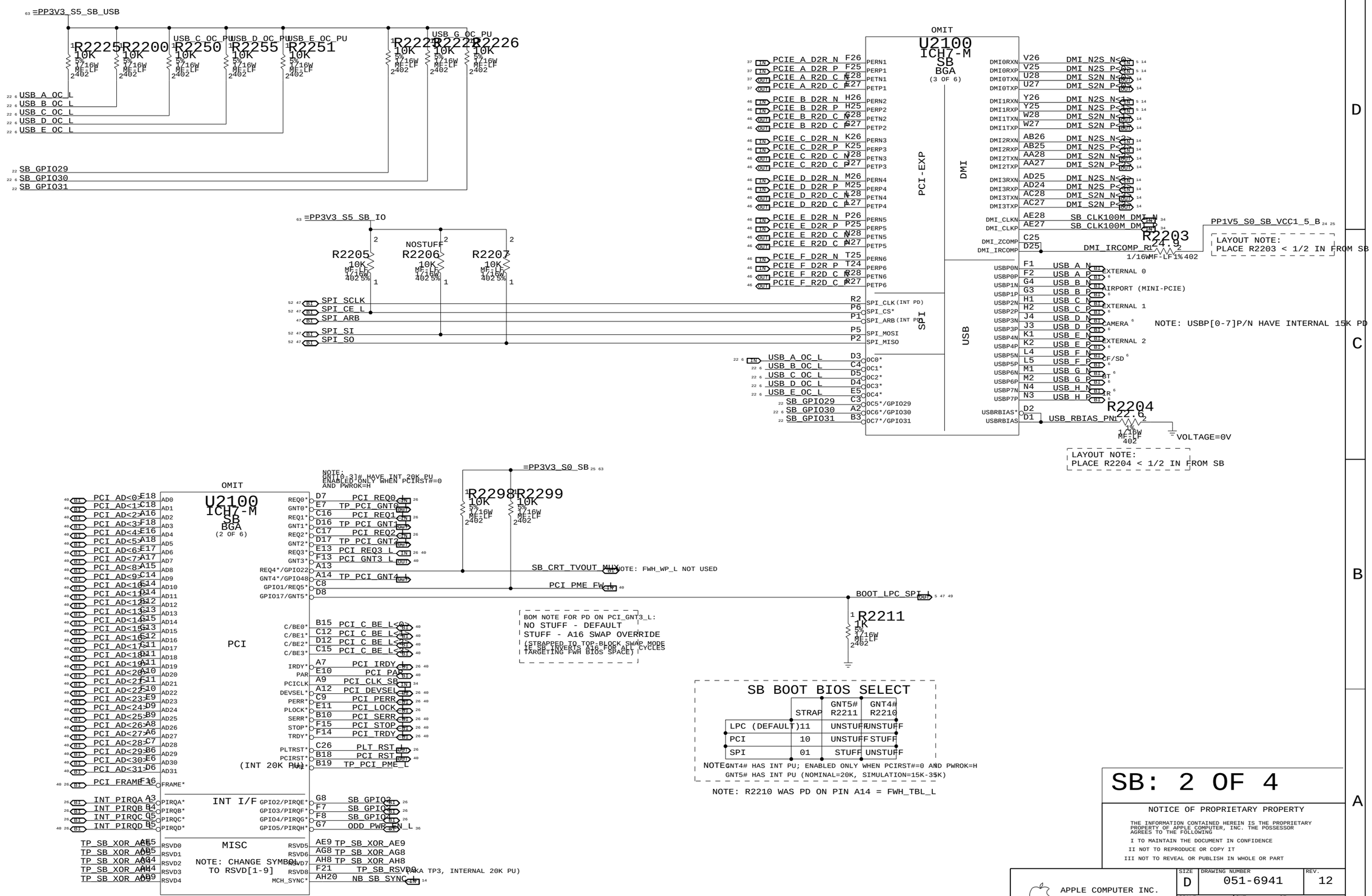
SCALE NONE	SHT 21 OF 104	



SB: 2 OF 4

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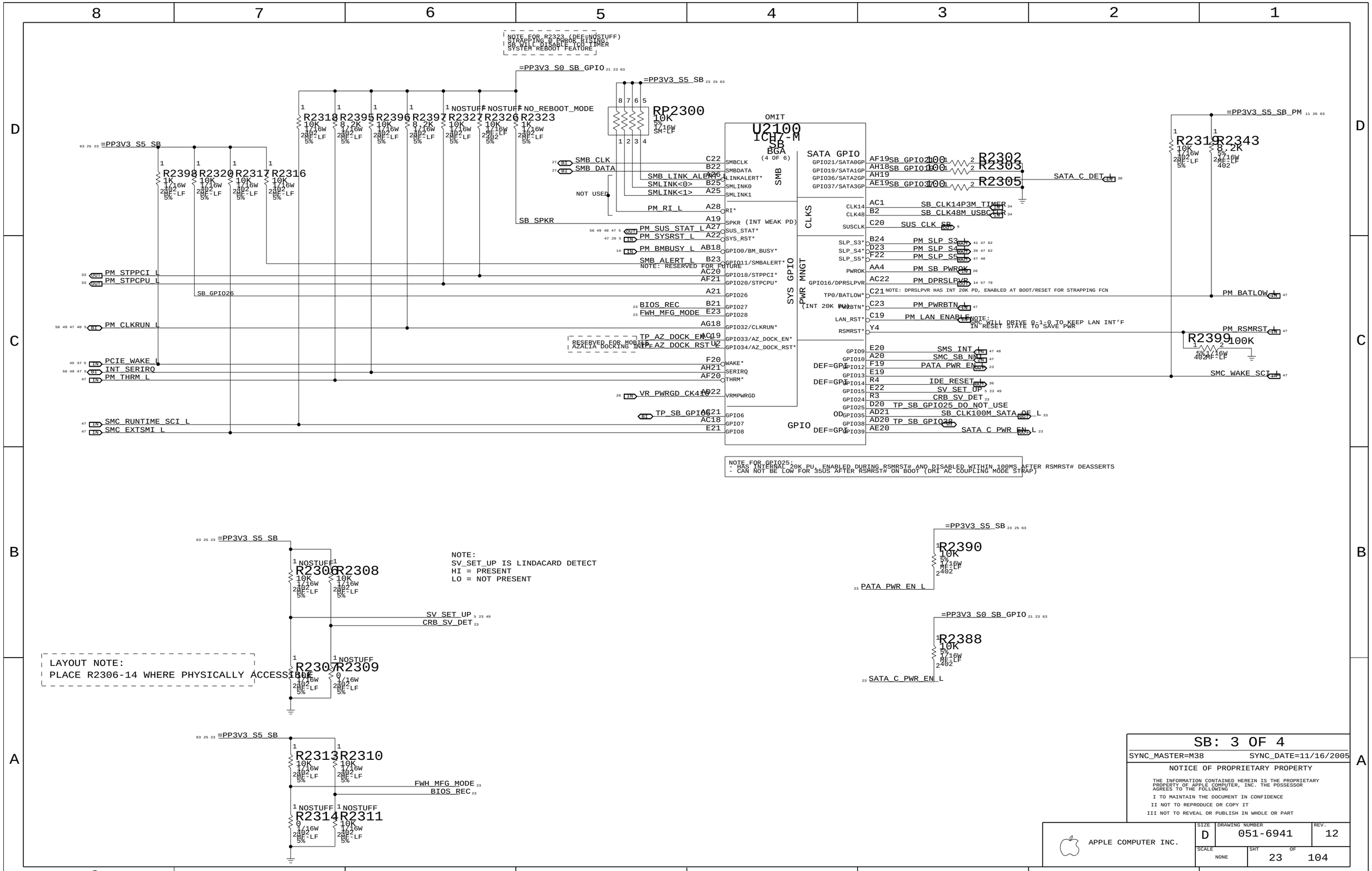
SCALE NONE | SHT 22 OF 104



SB: 3 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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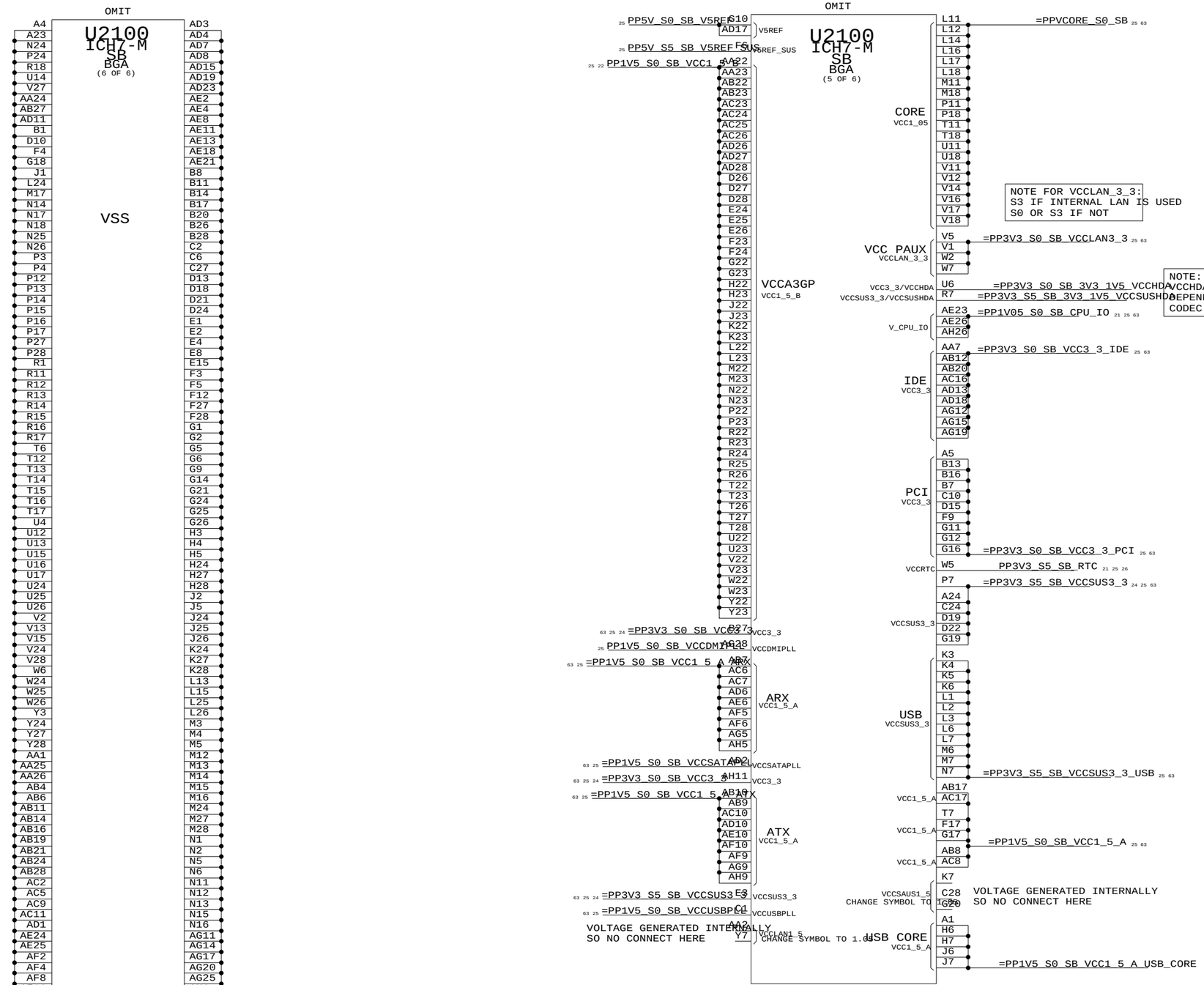
SCALE NONE | SHT 23 OF 104



SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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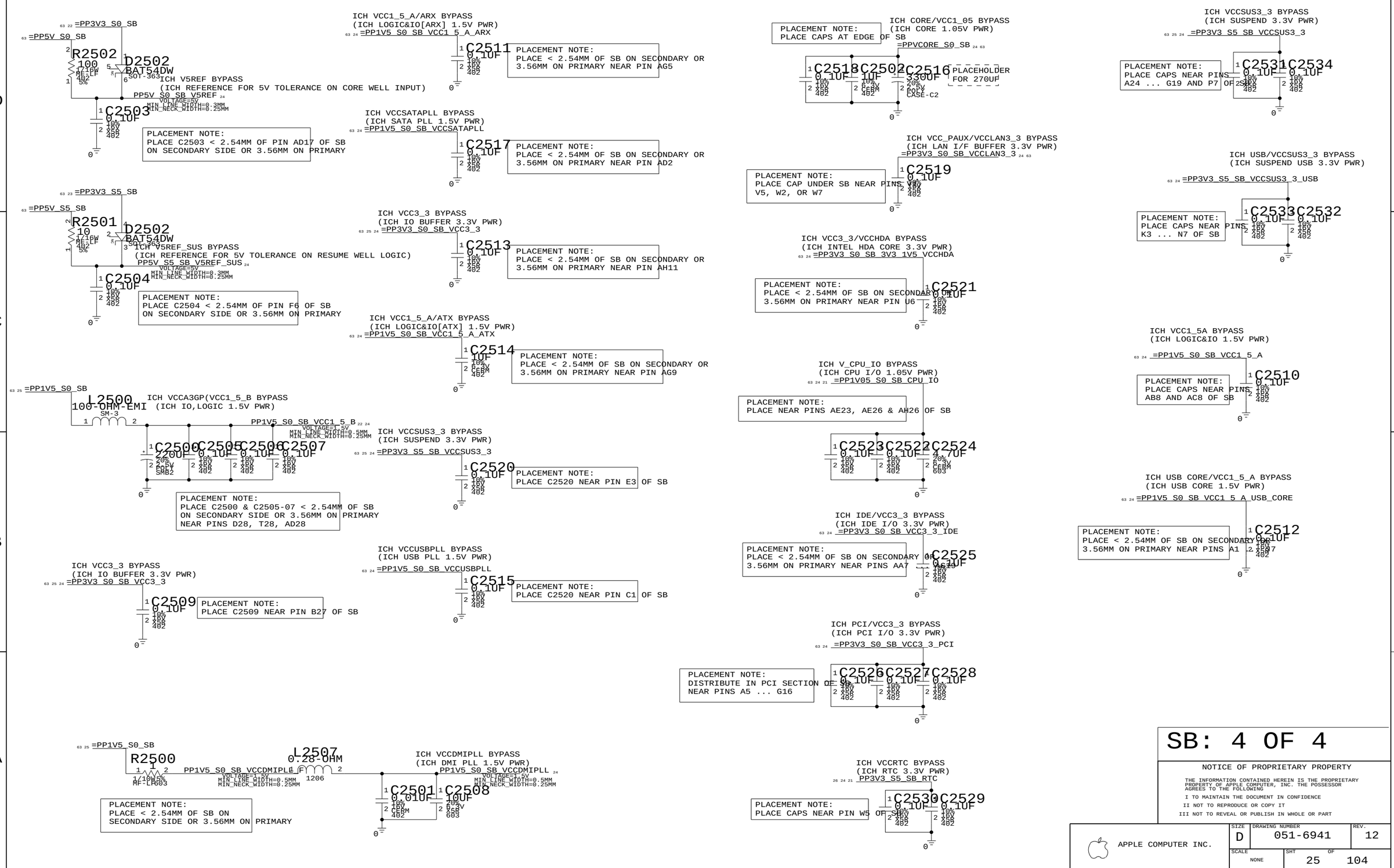
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE | SHT 24 OF 104


ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2511
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG5
=PP3V3_S0_SB
=PP5V_S0_SB
R2502
100
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503
0.1UF
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
=PP1V5_S0_SB_VCCSATAPLL
C2517
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AD2
=PP3V3_S5_SB
=PP5V_S5_SB
R2501
10
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504
0.1UF
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2513
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
C2514
1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG9
=PP1V5_S0_SB
L2500
100-OHM-EMI
SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500
22UF
20%
2.5V
POLY
SMB2
C2505
0.1UF
C2506
0.1UF
C2507
0.1UF
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2520
0.1UF
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
ICH VCCSUSPLL BYPASS
(ICH USB PLL 1.5V PWR)
=PP1V5_S0_SB_VCCUSBPLL
C2515
0.1UF
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2509
0.1UF
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
=PP1V5_S0_SB
R2500
1/10W5%
MF-LF003
L2507
0.28-OHM
1206
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2501
0.01UF
C2508
10UF
20%
6.3V
X6S
603
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
=PPVCORE_S0_SB
C2518
0.1UF
C2502
1UF
C2516
330UF
20%
2.5V
POSCAP
CASE-C2
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCCLAN3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS W6,
V5, W2, OR W7
C2519
0.1UF
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
=PP3V3_S0_SB_3V3_1V5_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
C2521
0.1UF
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
=PP1V05_S0_SB_CPU_IO
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523
0.1UF
C2522
0.1UF
C2524
4.7UF
20%
6.3V
X6S
603
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
C2525
0.1UF
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526
0.1UF
C2527
0.1UF
C2528
0.1UF
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
=PP3V3_S5_SB_RTC
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530
0.1UF
C2529
0.1UF
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531
0.1UF
C2534
0.1UF
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533
0.1UF
C2532
0.1UF
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510
0.1UF
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1
C2512
0.1UF
SB: 4 OF 4
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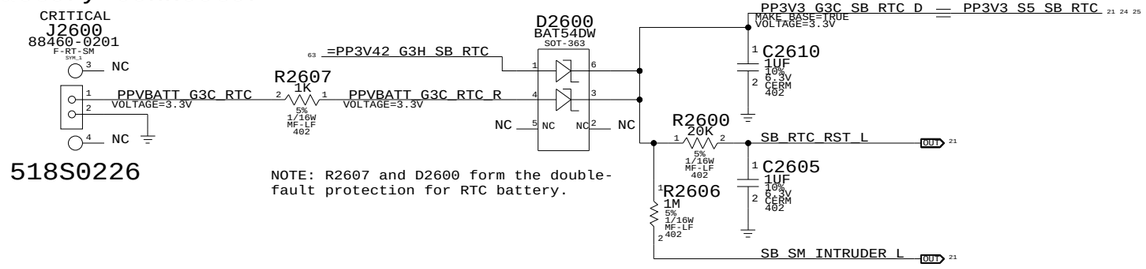
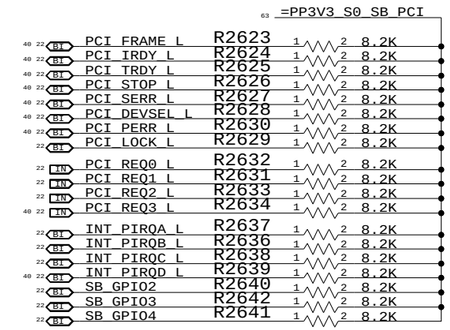
SIZE
D
DRAWING NUMBER
051-6941
REV.
12
SCALE
NONE
SHT
25
OF
104

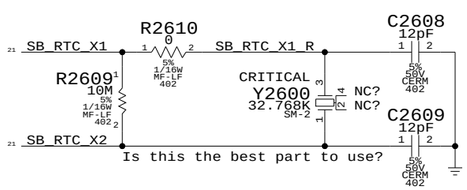
RTC Battery Connector



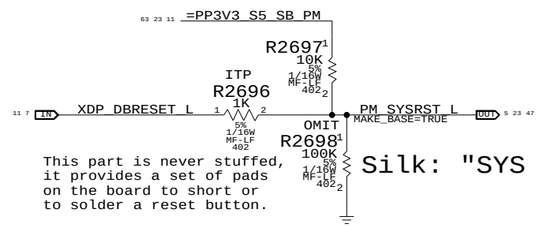
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



Is this the best part to use?

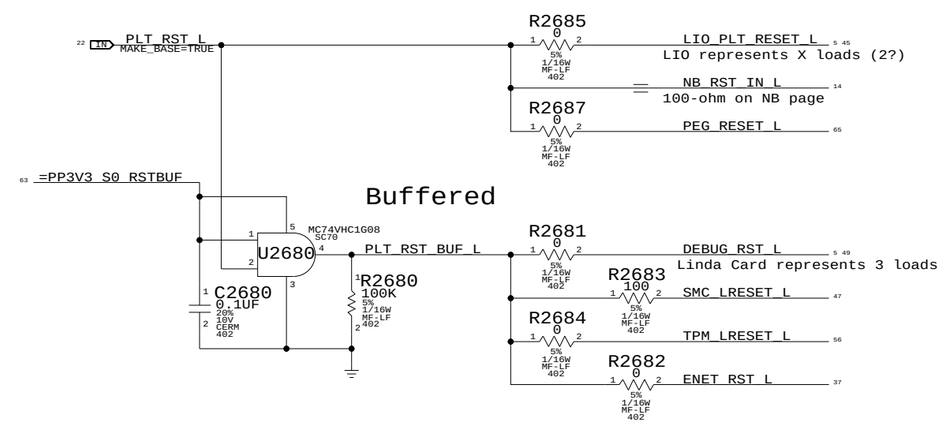


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

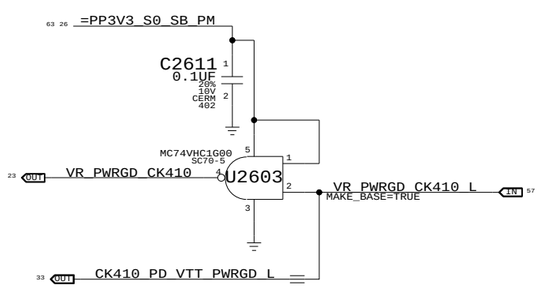
Silk: "SYS RST"

Platform Reset Connections

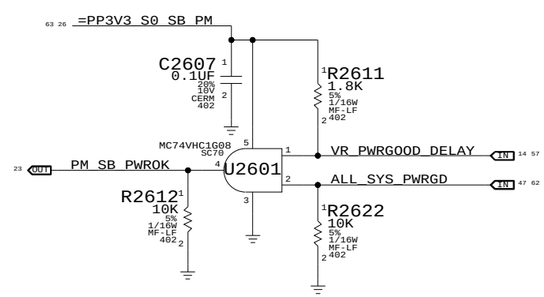
Unbuffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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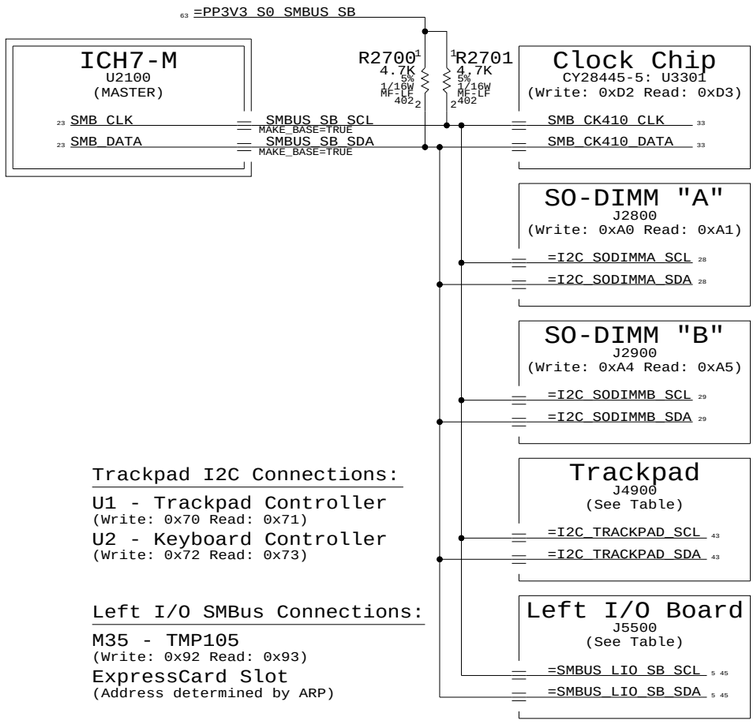
SCALE NONE	SHT 26 OF 104	

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

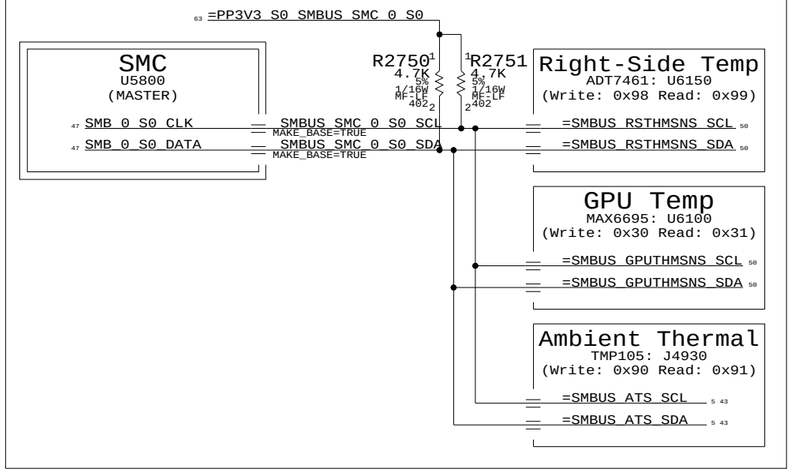
U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

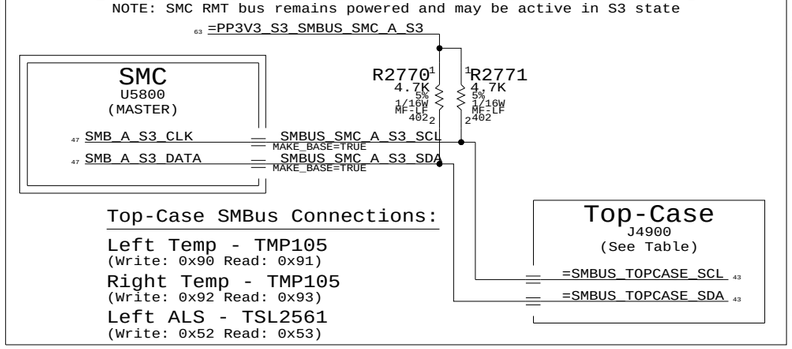
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



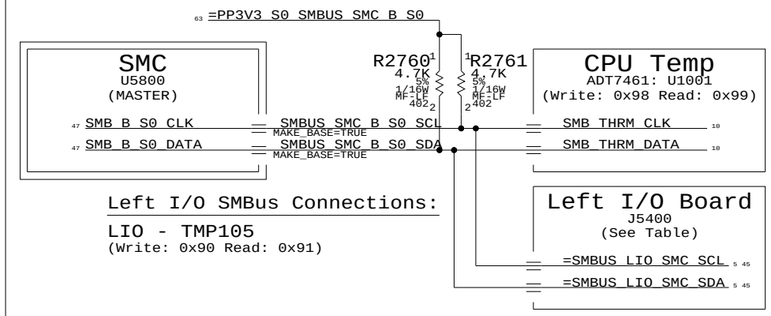
Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

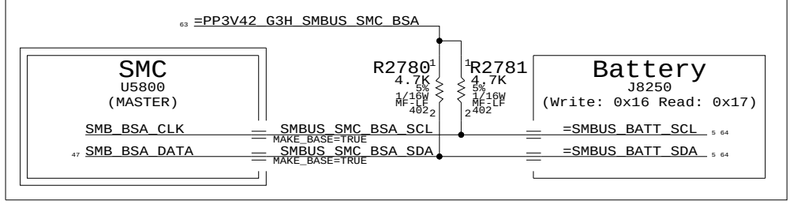
SMC "B" SMBus Connections



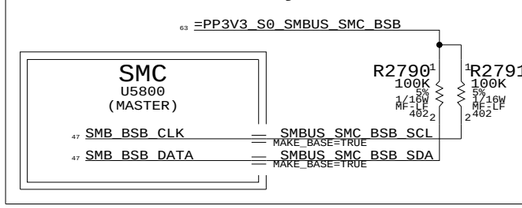
Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE | SHT 27 OF 104

Page Notes

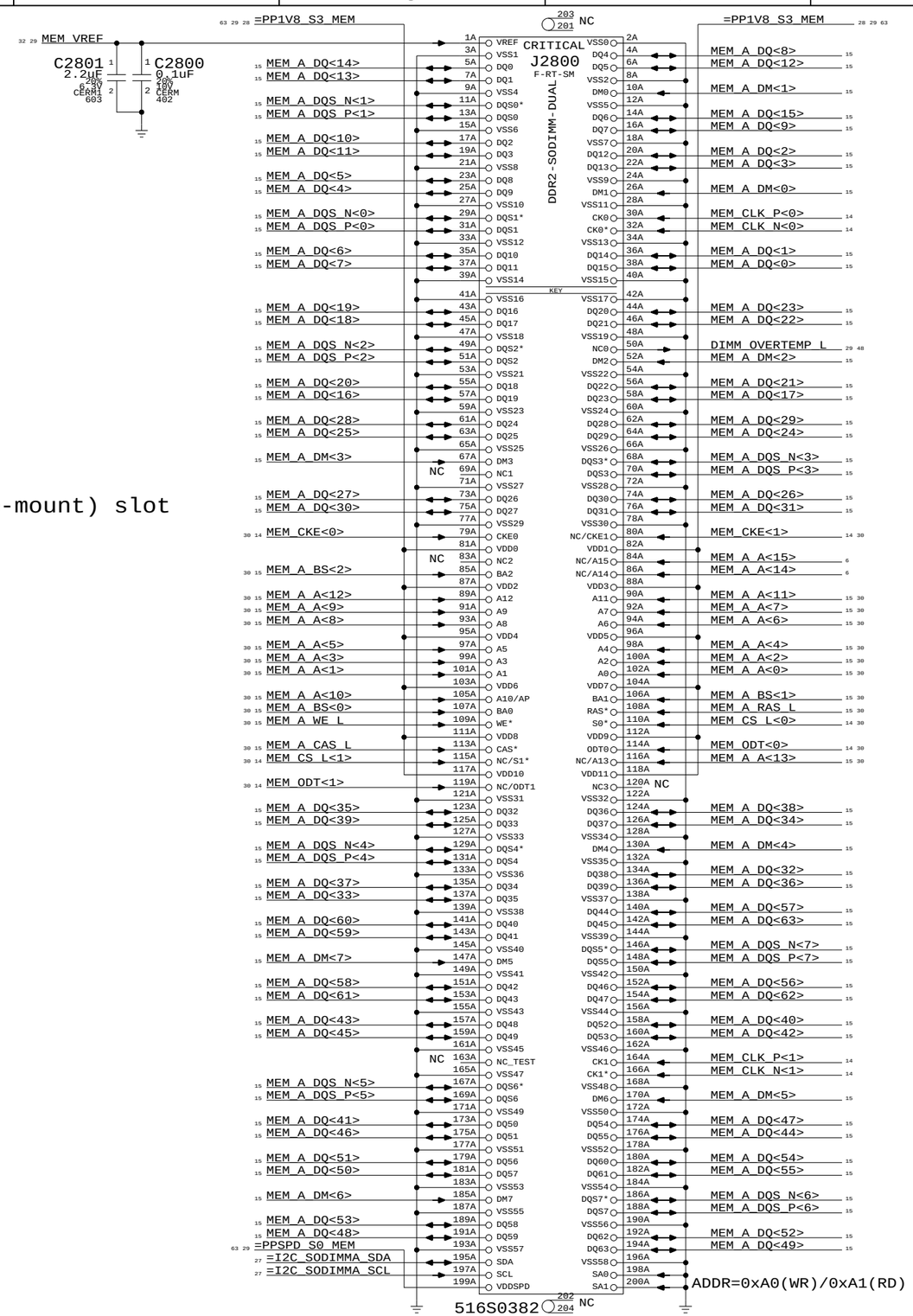
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

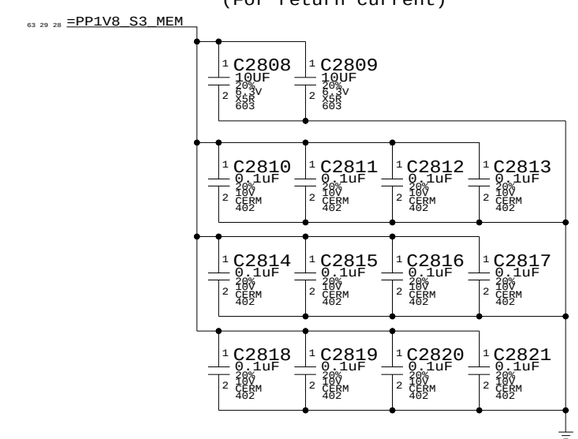
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Lower" (surface-mount) slot



DDR2 Bypass Caps
(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 28 OF 104	

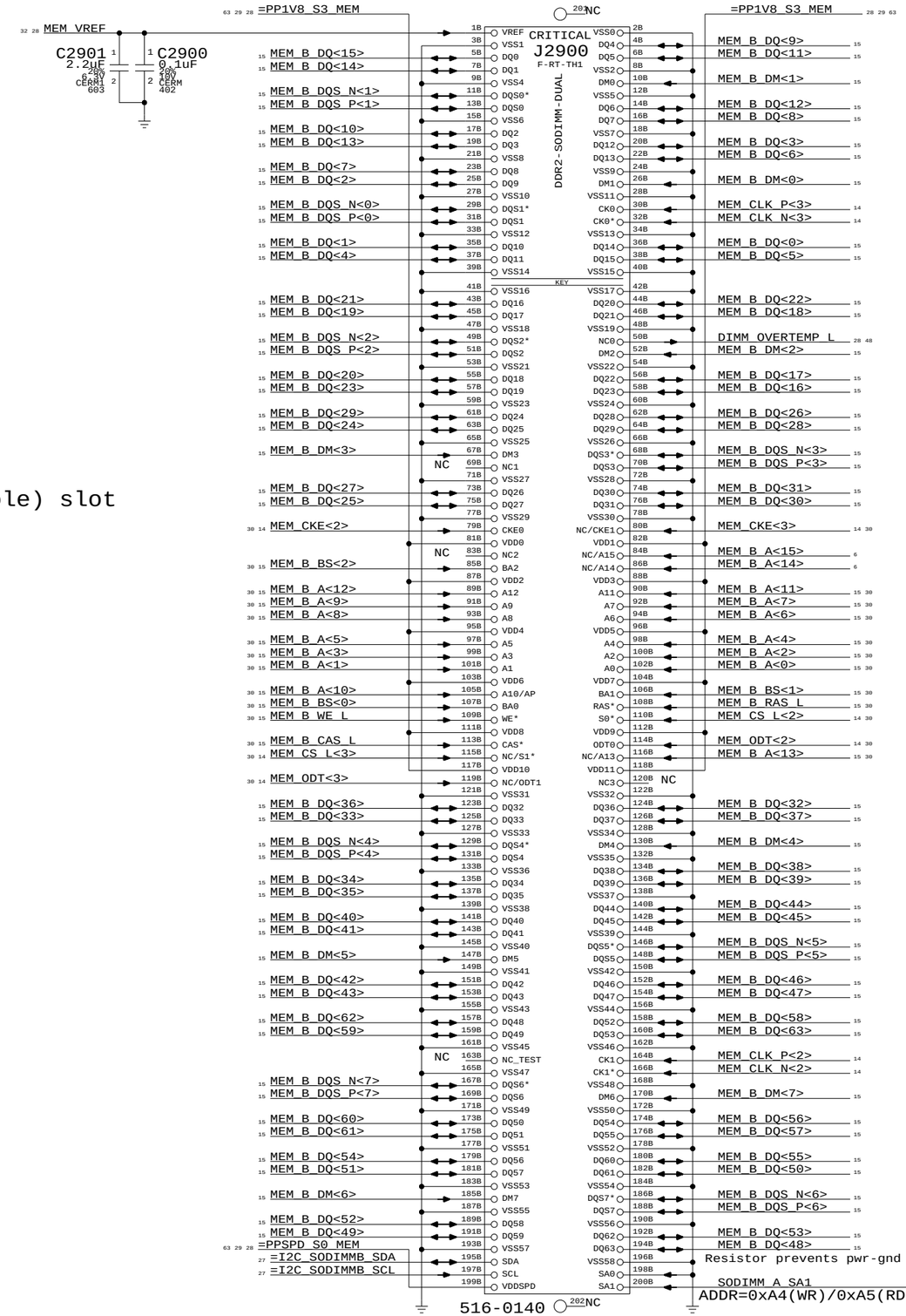
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

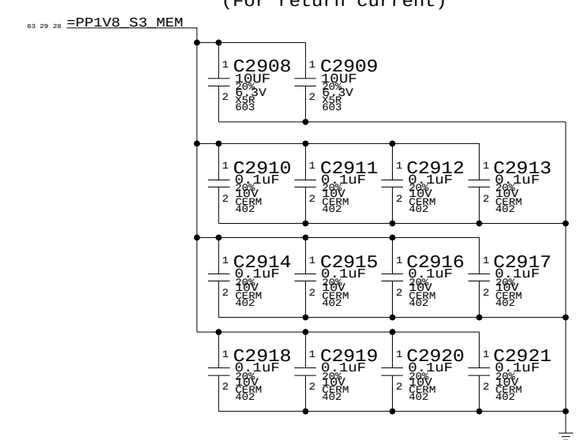
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.



"Upper" (thru-hole) slot

DDR2 Bypass Caps
(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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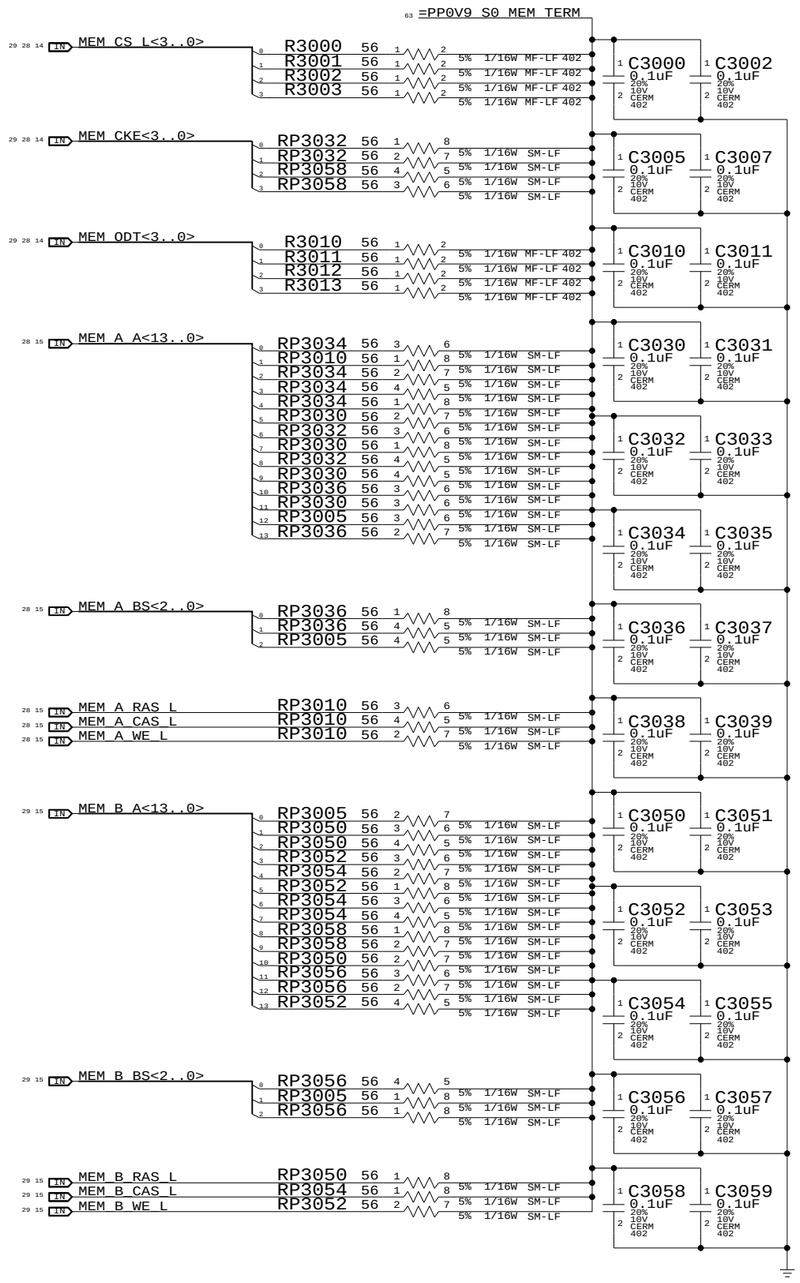
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE SHT 30 OF 104

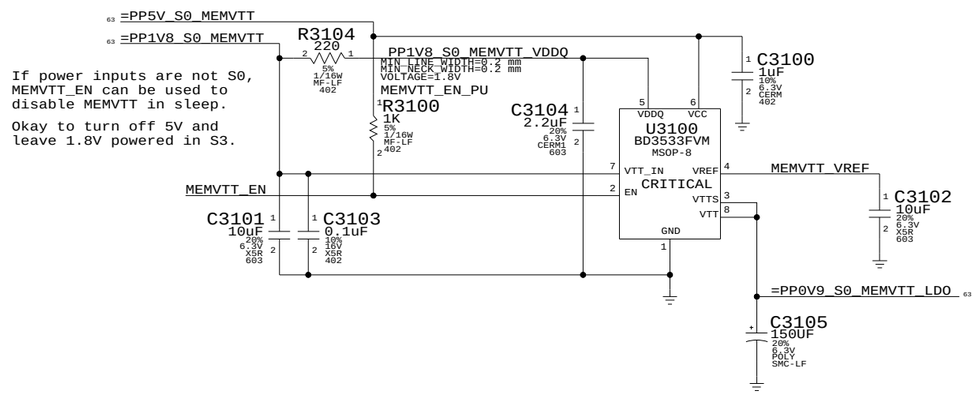
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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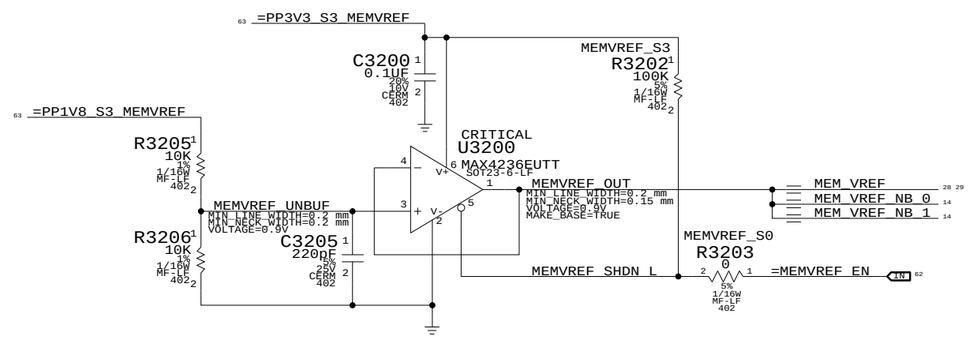
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE | SHT 31 OF 104



DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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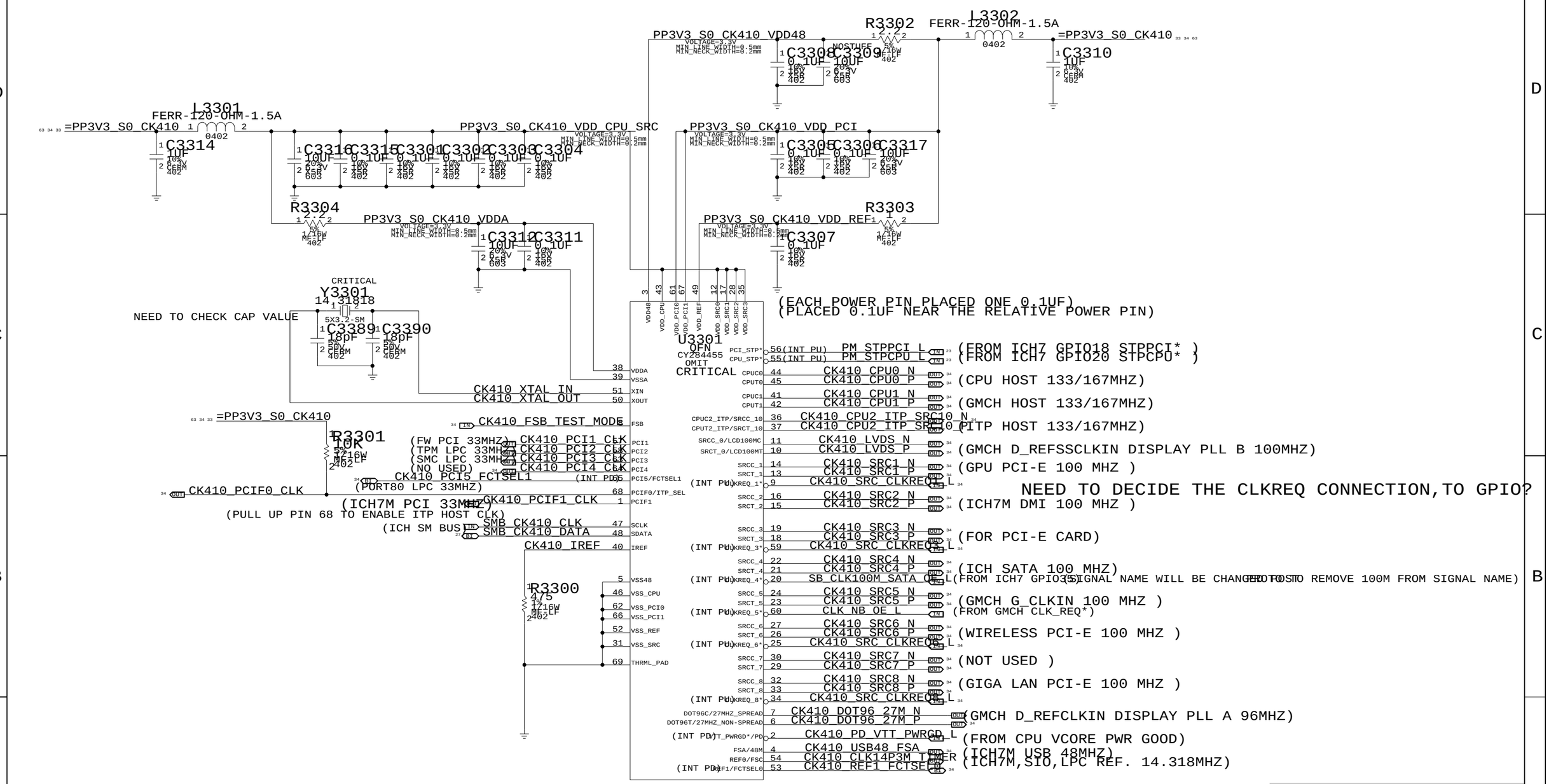
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	32	104



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_S	ST100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M52 SYNC_DATE=10/12/2005

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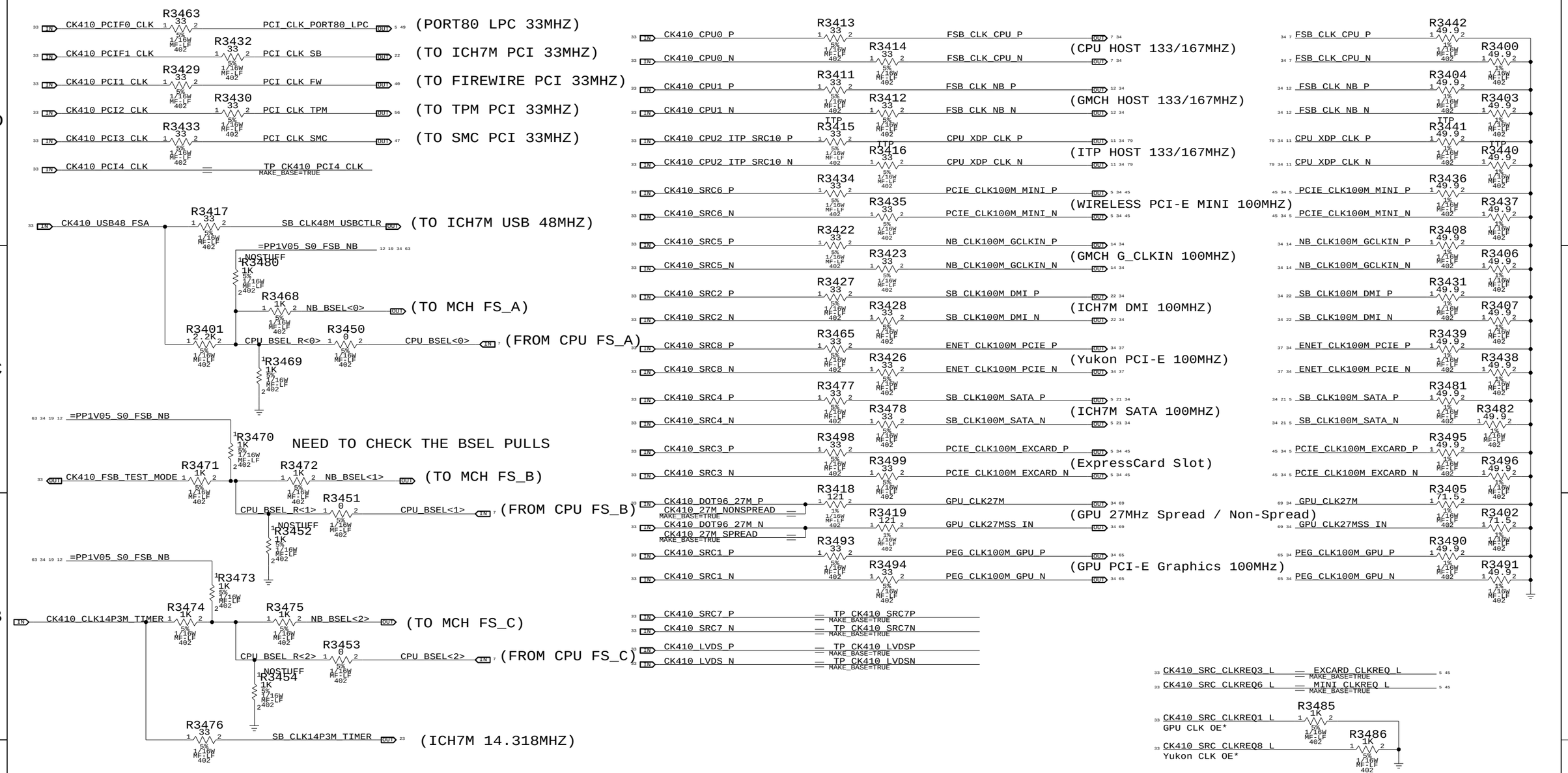
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE | SHT 33 OF 104



NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

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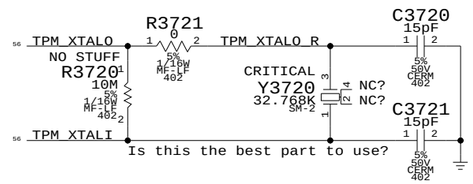
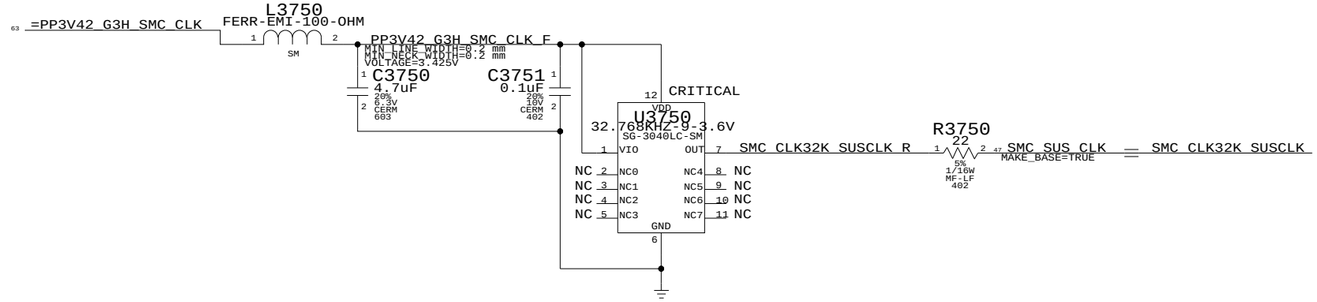
TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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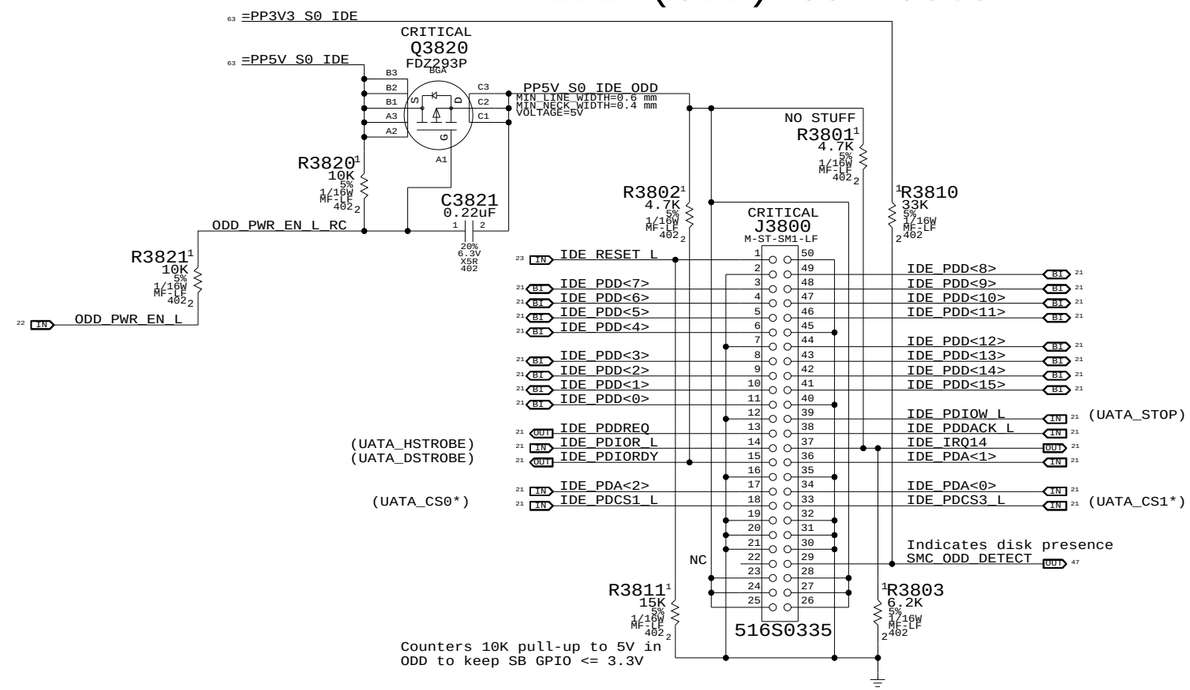
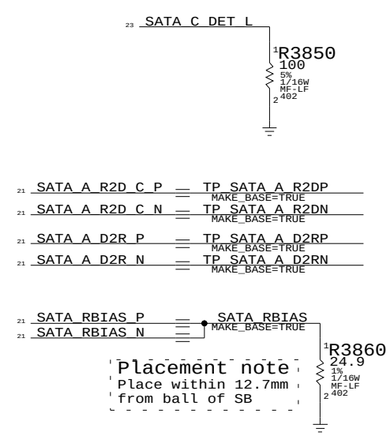
IDE (ODD) Connector





PATA Connector

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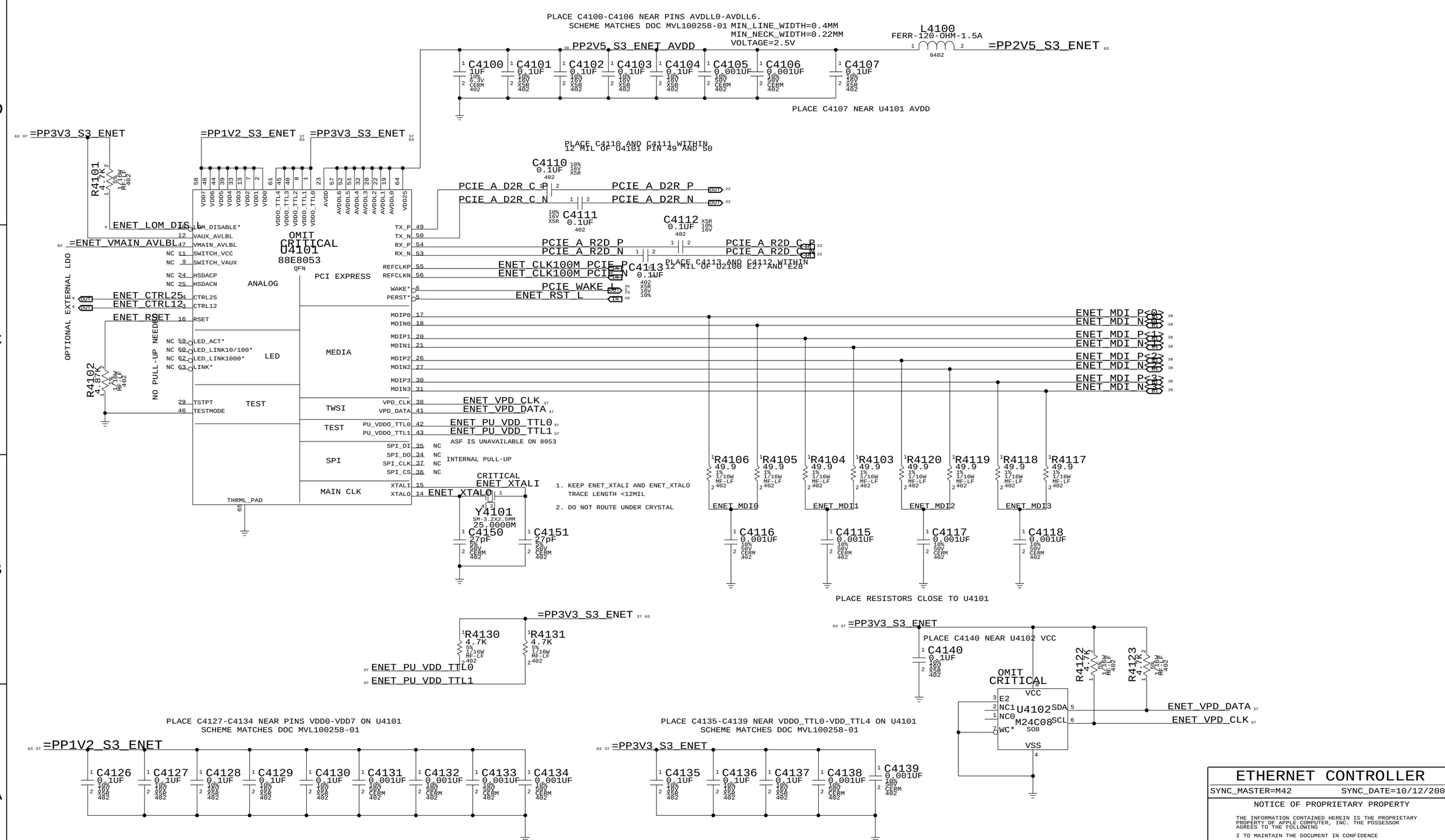
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 38 OF 104	



ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=10/12/2005

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APPLE COMPUTER INC.

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SCALE NONE SHT 41 OF 104

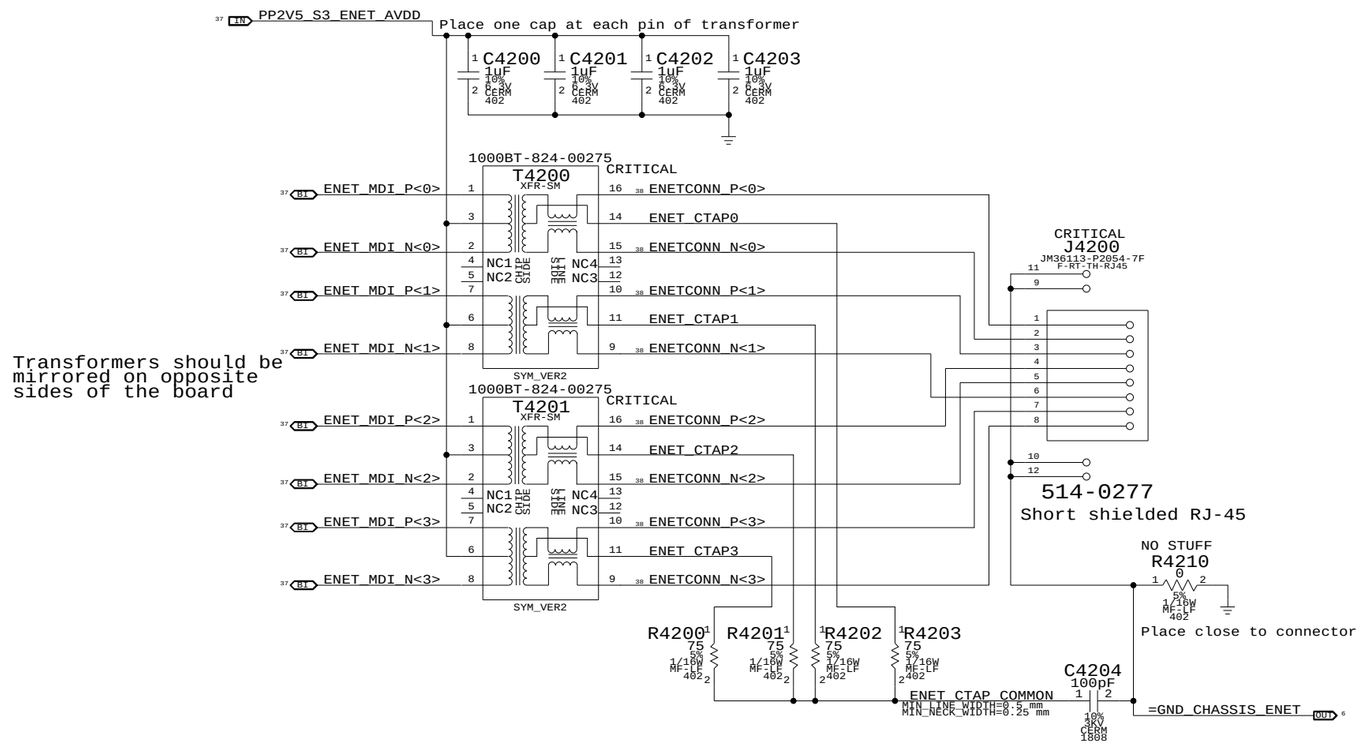
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 38
	ENETCONN	ENET_100D	ENETCONN_N<0> 38
	ENETCONN	ENET_100D	ENETCONN_P<1> 38
	ENETCONN	ENET_100D	ENETCONN_N<1> 38
	ENETCONN	ENET_100D	ENETCONN_P<2> 38
	ENETCONN	ENET_100D	ENETCONN_N<2> 38
	ENETCONN	ENET_100D	ENETCONN_P<3> 38
	ENETCONN	ENET_100D	ENETCONN_N<3> 38

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

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SIZE	DRAWING NUMBER	REV.
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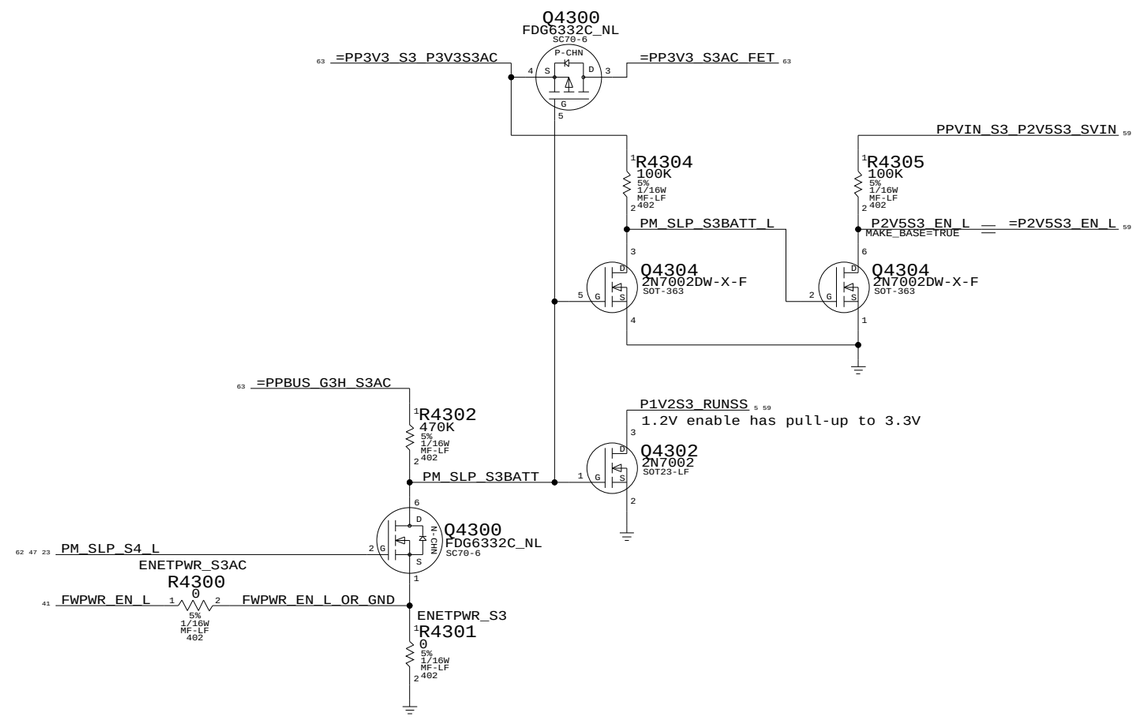
SCALE NONE	SHT 42	OF 104

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

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D	051-6941	12

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PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

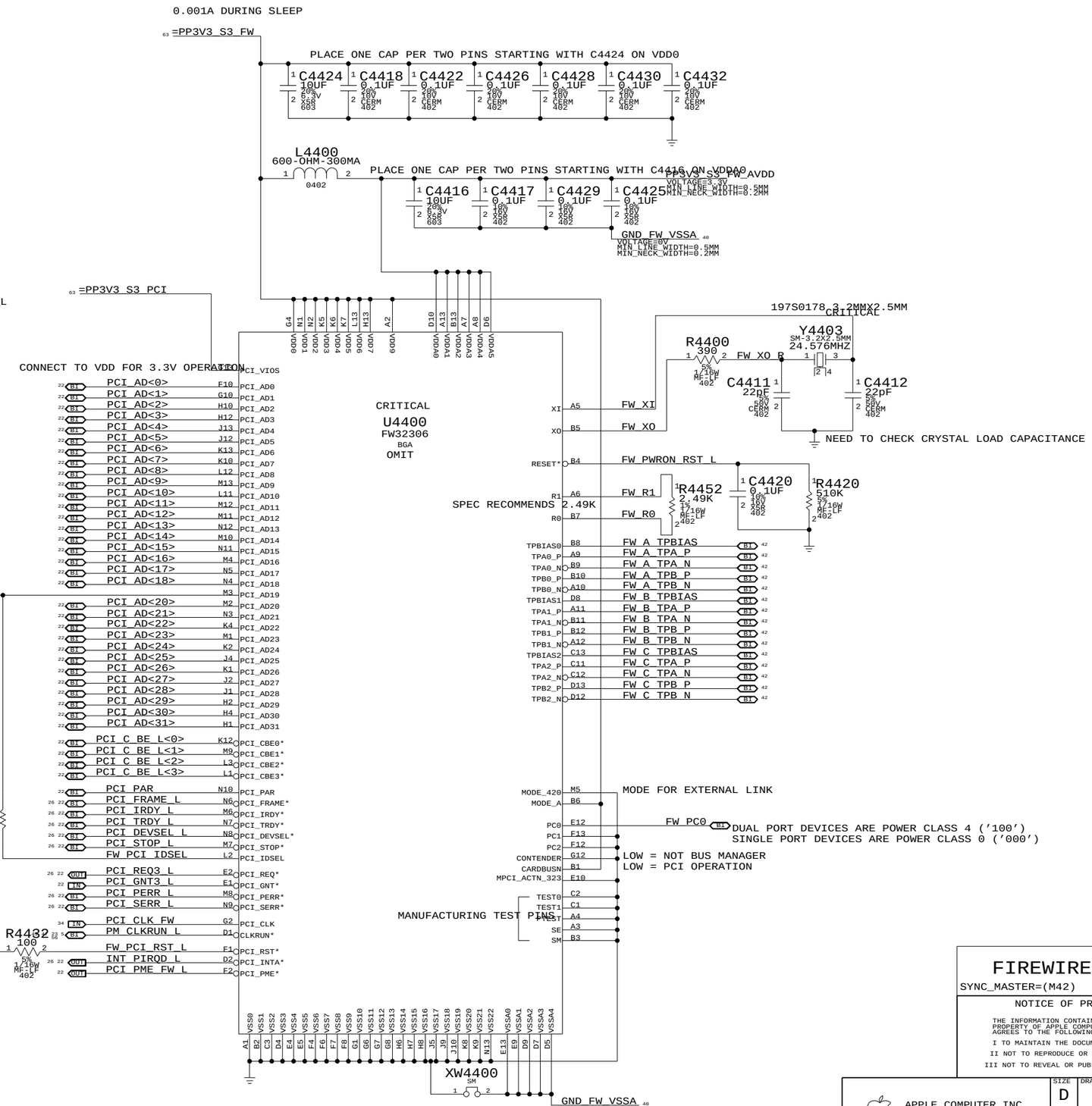
PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23506 ADDED
6/21/2005 - CHANGED INT*_TO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ_TO_TO_REQ3 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME_DIFF_PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND



FIRE WIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

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SCALE NONE	SHT 44 OF 104	

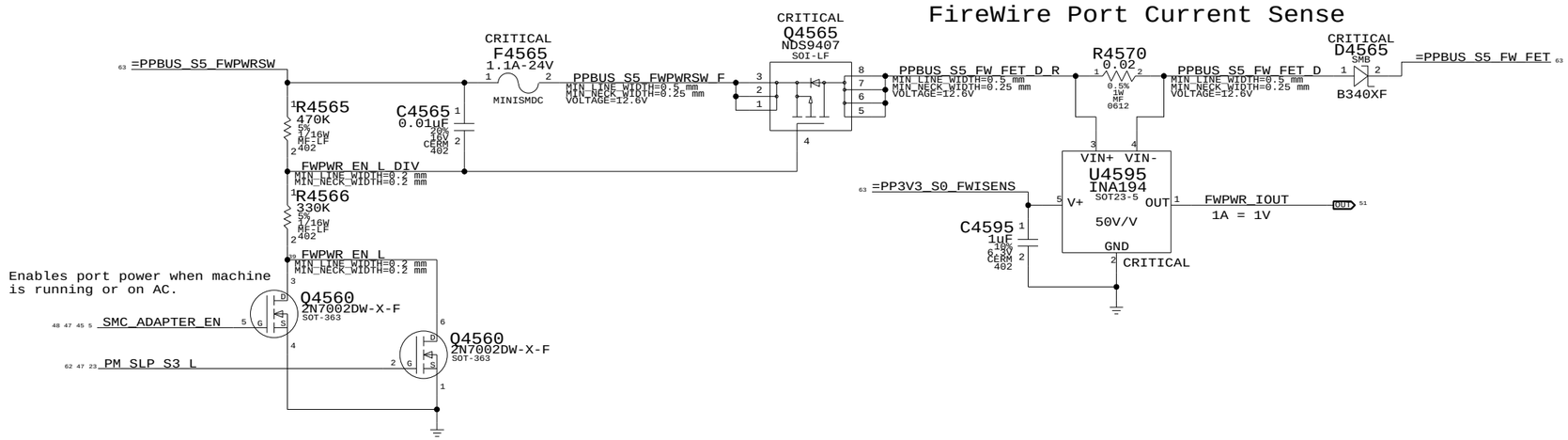
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



FireWire Port Current Sense

FireWire Port Power		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

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D	051-6941	12
SCALE NONE	SHT 45	OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED	FW	FW_110D	FW_PORT1_TPA_FL_P 42
BY	FW	FW_110D	FW_PORT1_TPA_FL_N 42
PHY	FW	FW_110D	FW_PORT1_TPB_FL_P 42
PAGE	FW	FW_110D	FW_PORT1_TPB_FL_N 42

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

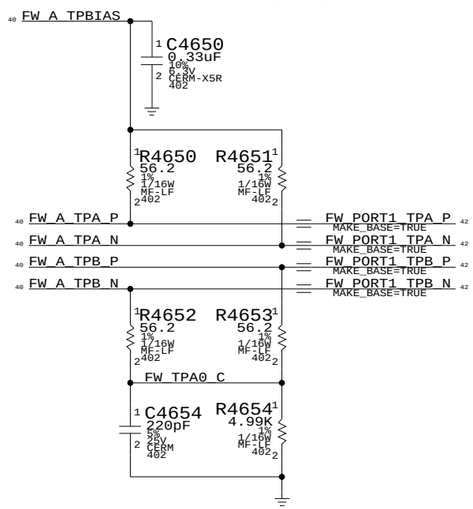
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

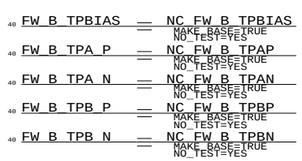
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

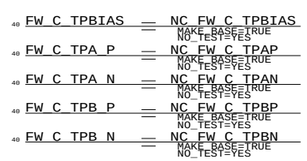
Place close to FireWire PHY



2nd TPA/TPB pair unused

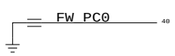


3rd TPA/TPB pair unused

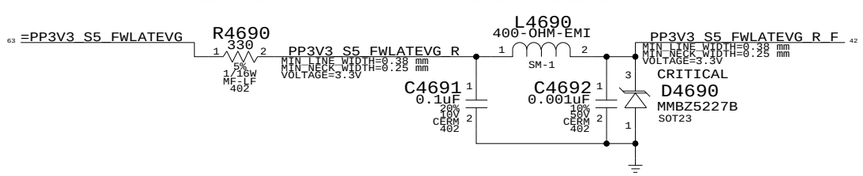


FW Power Class Strap

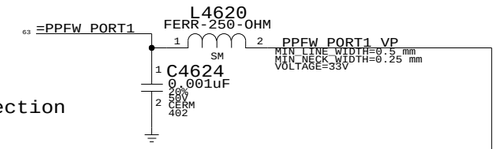
Single-port system sets PC=0



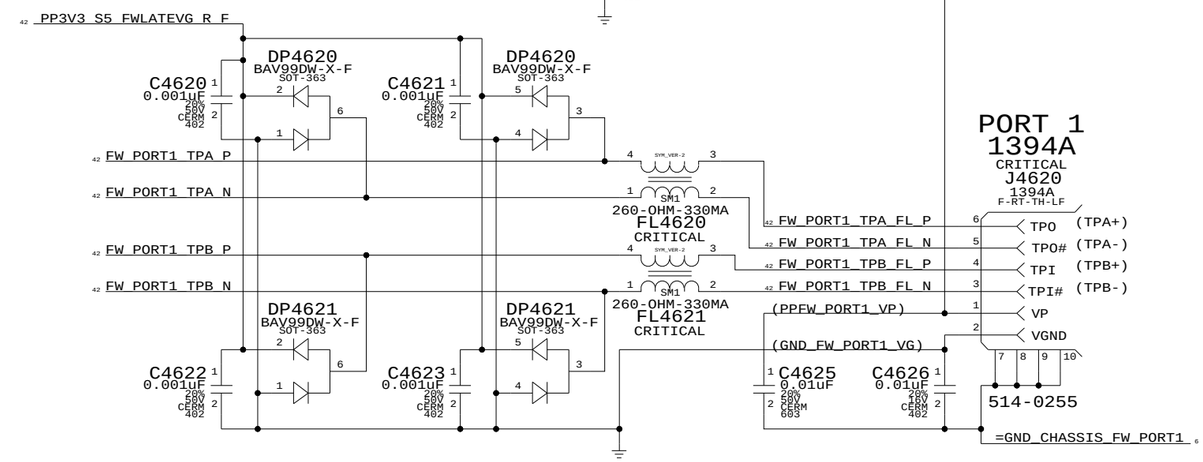
Late-VG Protection Power

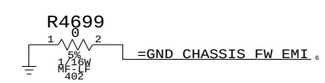


Cable Power



"Snapback" & "Late VG" Protection





FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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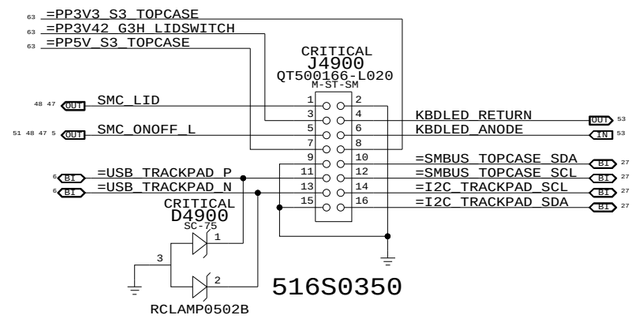
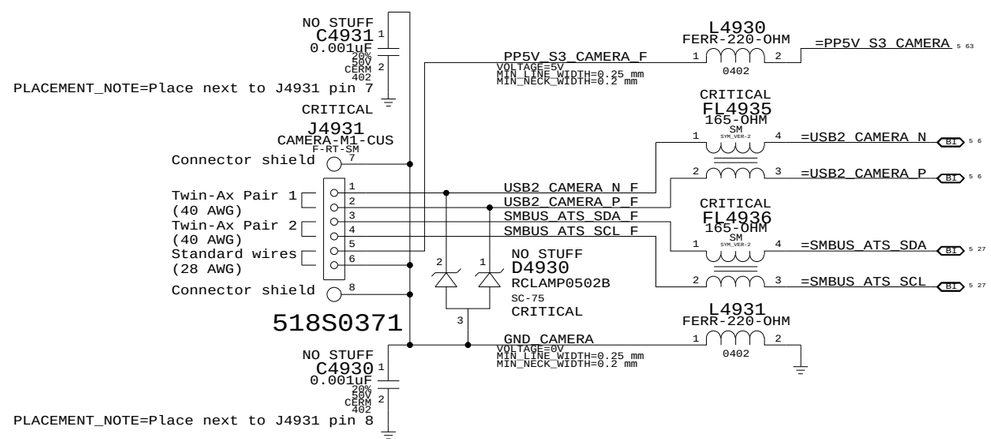
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 46 OF 104	

Top-Case Connector



Camera Connector



Internal USB Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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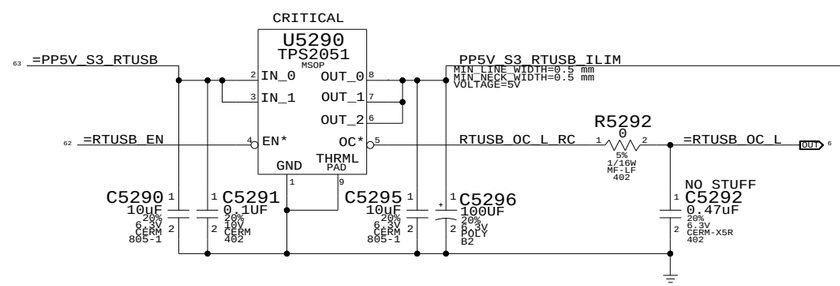
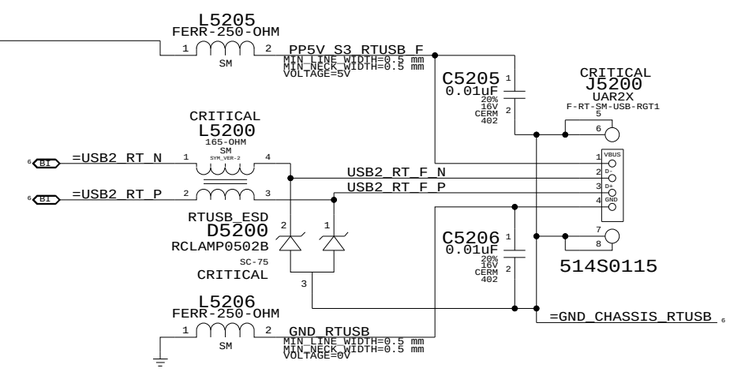
Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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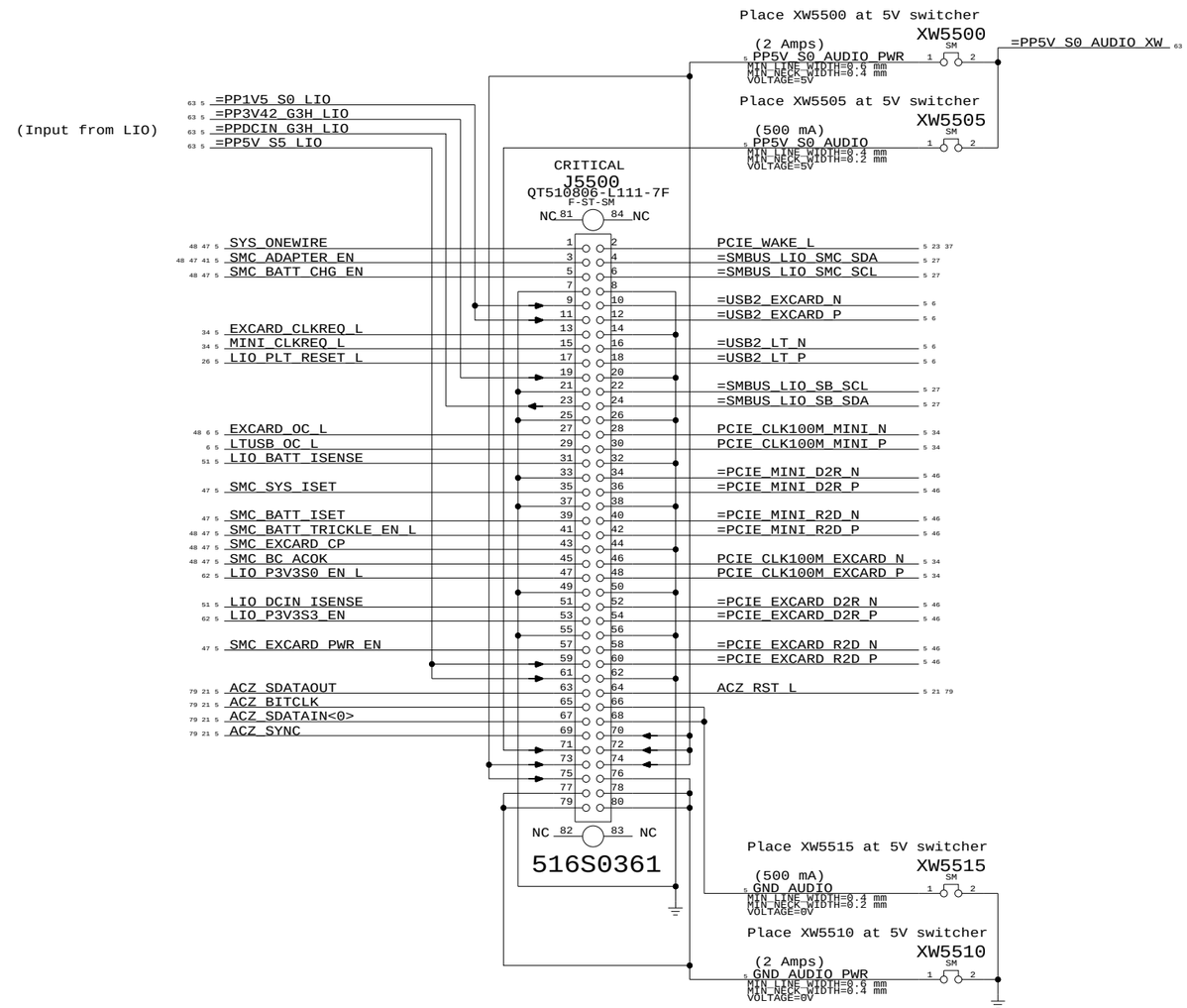
SCALE NONE	SHT 52 OF 104	

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE NONE

SHT 55 OF 104

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402

Place caps close to SB

45 5	=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P (MAKE_BASE=TRUE)	C5710 1 2	PCIE_B_R2D_C_P	22
45 5	=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N (MAKE_BASE=TRUE)	C5711 1 2	PCIE_B_R2D_C_N	22
45 5	=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P (MAKE_BASE=TRUE)		PCIE_B_D2R_P	22
45 5	=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N (MAKE_BASE=TRUE)		PCIE_B_D2R_N	22

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402

Place caps close to SB

45 5	=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE)	C5720 1 2	PCIE_C_R2D_C_P	22
45 5	=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE)	C5721 1 2	PCIE_C_R2D_C_N	22
45 5	=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE)		PCIE_C_D2R_P	22
45 5	=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE)		PCIE_C_D2R_N	22

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP (MAKE_BASE=TRUE)	PCIE_D_R2D_C_P	22
TP_PCIE_D_R2DN (MAKE_BASE=TRUE)	PCIE_D_R2D_C_N	22
TP_PCIE_D_D2RP (MAKE_BASE=TRUE)	PCIE_D_D2R_P	22
TP_PCIE_D_D2RN (MAKE_BASE=TRUE)	PCIE_D_D2R_N	22

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP (MAKE_BASE=TRUE)	PCIE_E_R2D_C_P	22
TP_PCIE_E_R2DN (MAKE_BASE=TRUE)	PCIE_E_R2D_C_N	22
TP_PCIE_E_D2RP (MAKE_BASE=TRUE)	PCIE_E_D2R_P	22
TP_PCIE_E_D2RN (MAKE_BASE=TRUE)	PCIE_E_D2R_N	22

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP (MAKE_BASE=TRUE)	PCIE_F_R2D_C_P	22
TP_PCIE_F_R2DN (MAKE_BASE=TRUE)	PCIE_F_R2D_C_N	22
TP_PCIE_F_D2RP (MAKE_BASE=TRUE)	PCIE_F_D2R_P	22
TP_PCIE_F_D2RN (MAKE_BASE=TRUE)	PCIE_F_D2R_N	22

PCI-E Connections

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UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	SPI_ARB
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	SPI_SCLK
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	SPI_SI
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	SPI_SO
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT_3_3_L
SMC_P20	D13	P20	P70/AN0	N12	SMC_CPU_ISENSE
SMC_P21	D14	P21	P71/AN1	R13	SMC_CPU_VSENSE
SMC_P22	D15	P22	P72/AN2	P13	SMC_GPU_ISENSE
SMC_P23	E12	P23	P73/AN3	R14	SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE
SMC_P26	E13	P26	P76/AN6	N13	SMC_BATT_ISENSE
SMC_P27	F14	P27	P77/AN7	P15	SMC_FWIRE_ISENSE
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	SMC_TPM_GPIO
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SC_TX_L
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SC_RX_L
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L
SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	SMC_BC_ACOK
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	PM_SLP_S4_L
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	SMC_SUS_CLK
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	SMB_0_S0_DATA
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1			
SMC_TX_L	G1	P50			
SMC_RX_L	G4	P51			
SMB_0_S0_CLK	F2	P52/SCL0			

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2BC	PE0	M3	SMC_CASE_OPEN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2BD	PE1*/ETCK	M2	SMC_TCK
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	SMC_BATT_VSET
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	SMC_SYS_VSET
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SPI_CE_L
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	SMB_BSA_DATA
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	SMB_BSA_CLK
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	SMB_A_S3_DATA
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	SMB_A_S3_CLK
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	SMB_B_S0_DATA
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	SMB_B_S0_CLK
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	SMS_INT_L
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	SMS_ONOFF_L
SMC_ANALOG_ID	N11	PD3/AN11			
SMC_NB_ISENSE	P10	PD4/AN12			
SMC_MEM_ISENSE	R10	PD5/AN13			
ALS_LEFT	N10	PD6/AN14			
ALS_RIGHT	M10	PD7/AN15			

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

=PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402

VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

=PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.20
MIN_NECK_WIDTH=0.20
C5820 0.1UF 20% 10V CERM 402

PP3V3_AVREF_SMC
=PP3V3_S5_SMC

OMIT
U5800
SMC_H8S2116
BGA
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GND_SMC_AVSS

SMC_RST_L	E3	RES*	
SMC_XTAL	A2	XTAL	
SMC_EXTAL	B2	EXTAL	
	E2	MD1	SMC_MD1
	K1	MD2	KBC_MDE
	F4	NMI	SMC_NMI
	L1	ETRST*	SMC_TRST_L
	P12	AVSS	
	R12	AVSS	

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
R5898 10K 5% 1/16W MF-LF 402
R5803 10K 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
NOSTUFF

XW5800
SM
GND_SMC_AVSS

SMC

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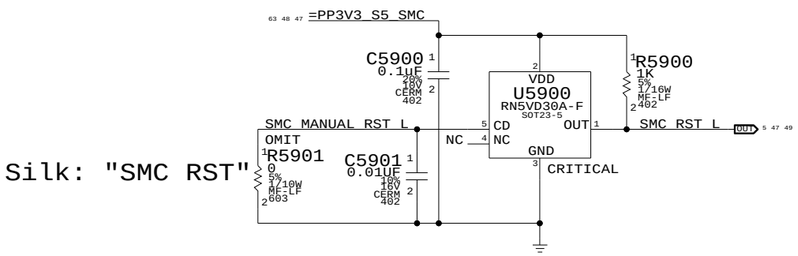
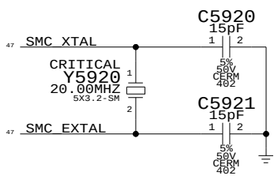
SCALE NONE	SHT 58 OF 104	

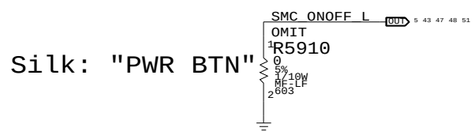
SMC Reset Button / Brownout Detect



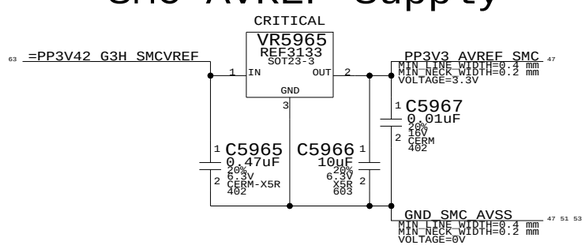
SMC Crystal Circuit



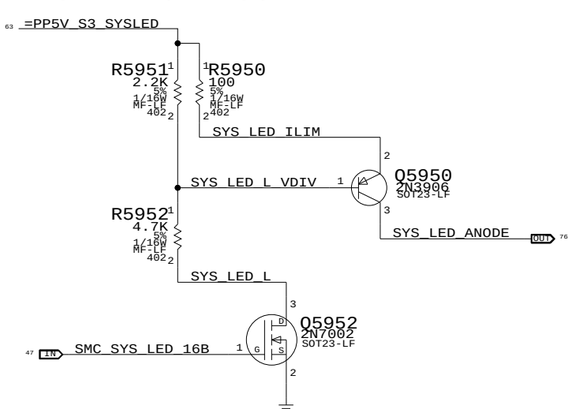
Debug Power Button

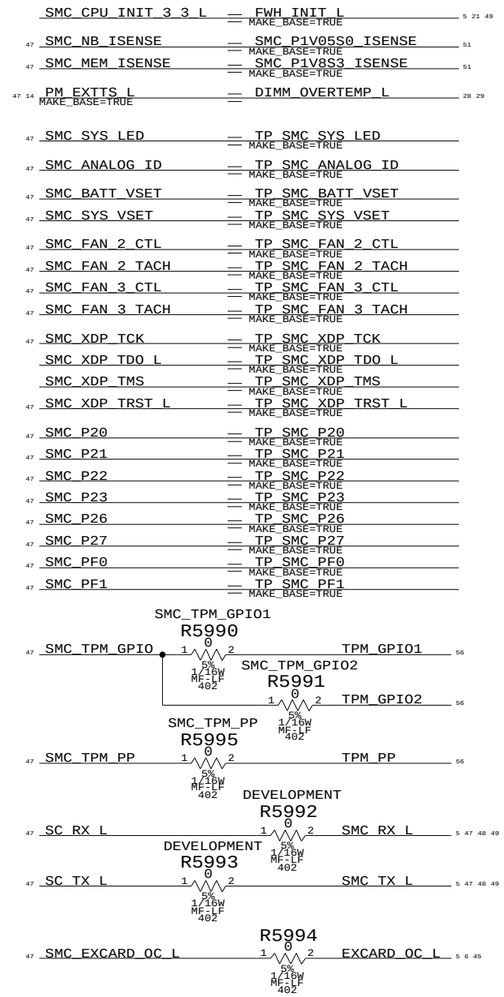


SMC AVREF Supply



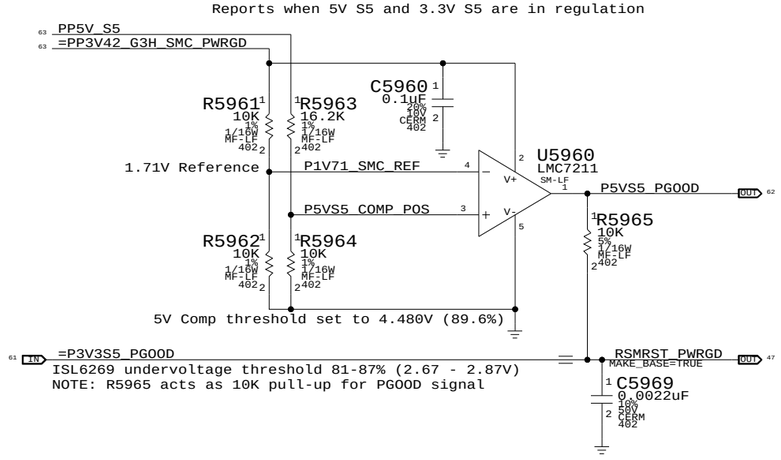
System (Sleep) LED Circuit



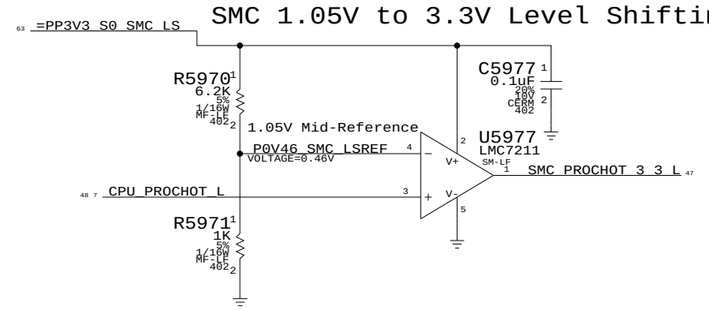


SMC PWRGD Circuit

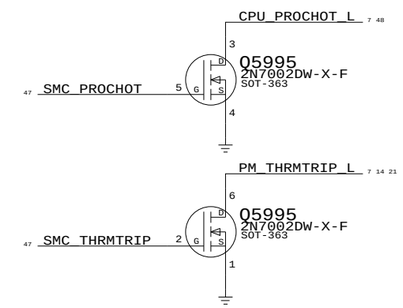
Reports when 5V S5 and 3.3V S5 are in regulation

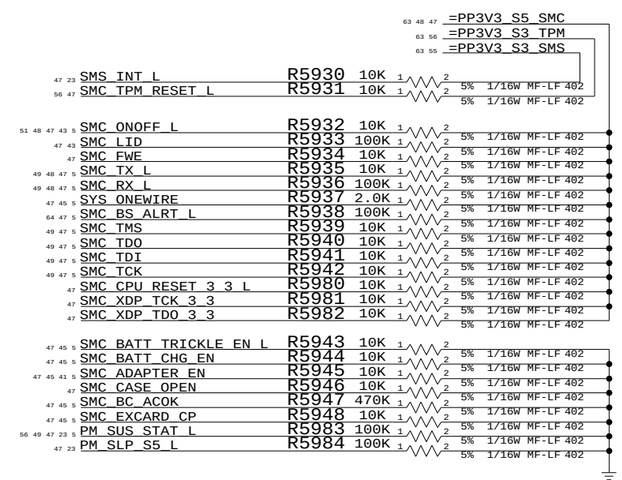


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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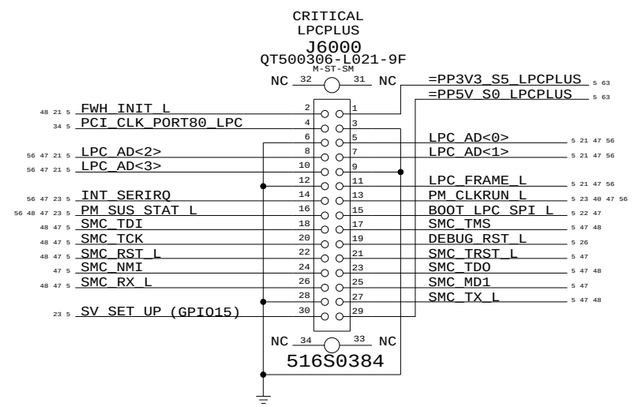
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 59 OF 104	



LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

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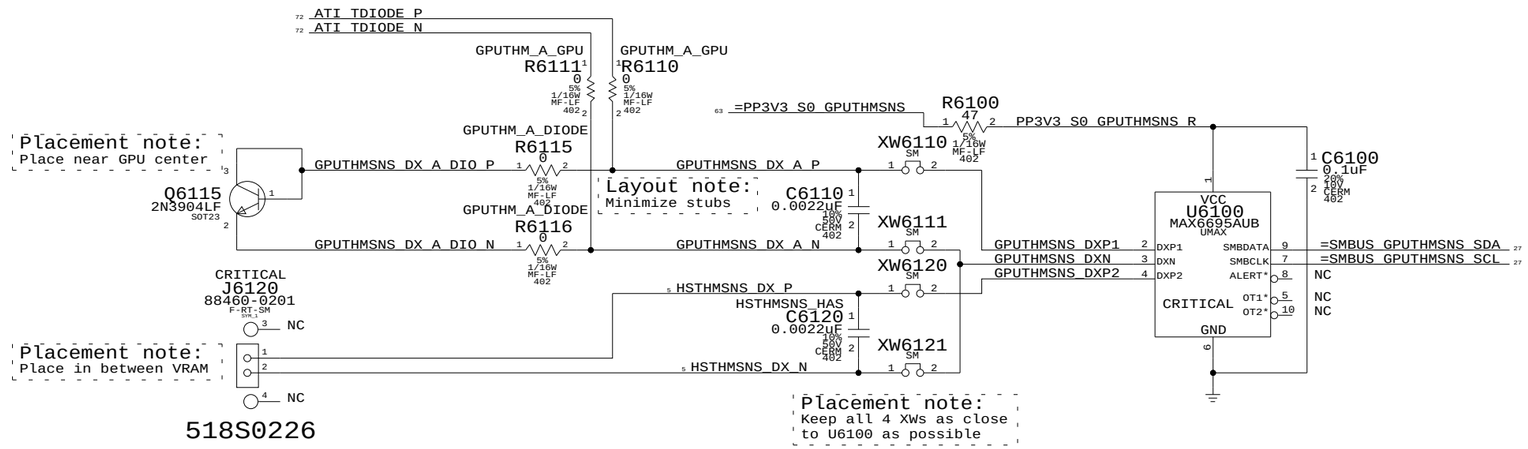
D	051-6941	12

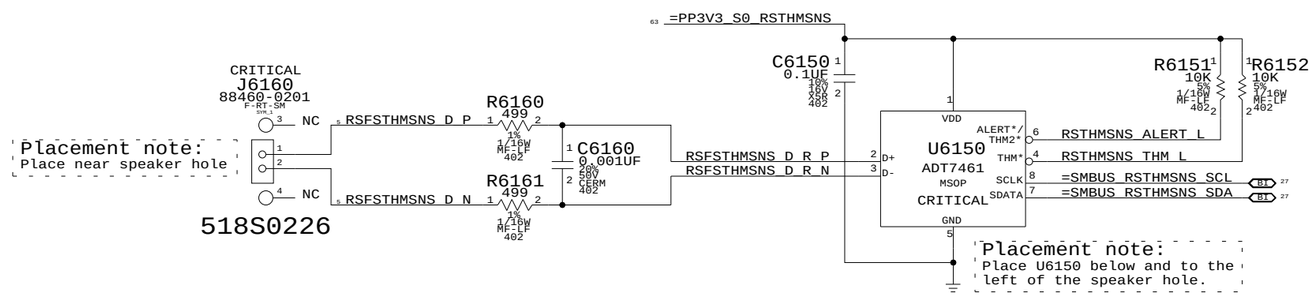
SCALE	SHT	OF
NONE	60	104

GPU / Heat Pipe Thermal Sensor

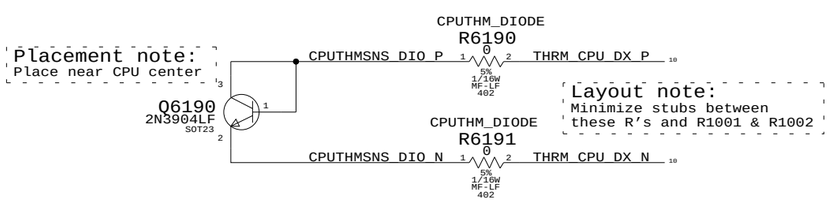


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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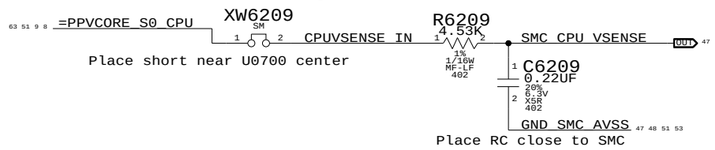
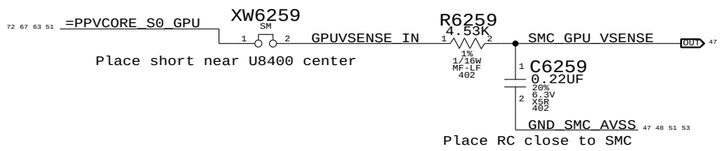
D	051-6941	12

SCALE NONE | SHT 61 OF 104

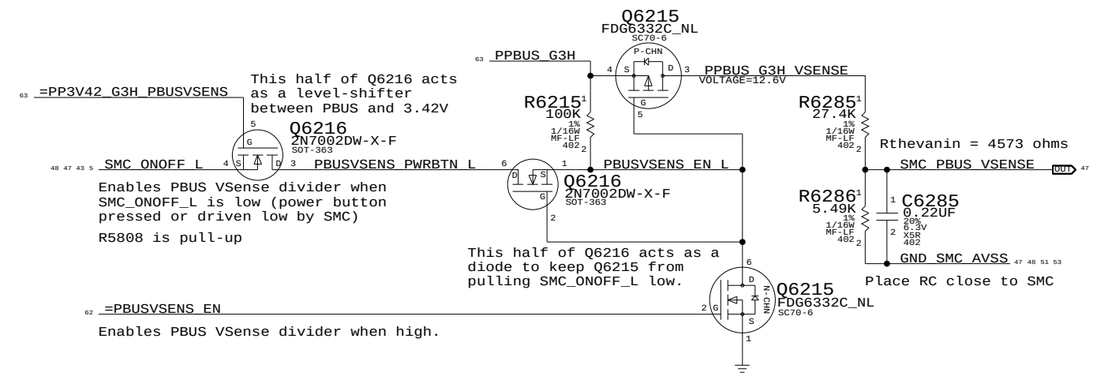
CPU Voltage Sense / Filter



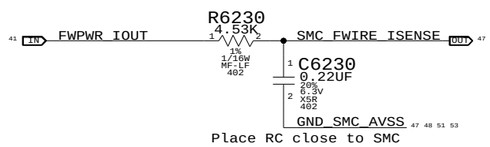
GPU Voltage Sense / Filter



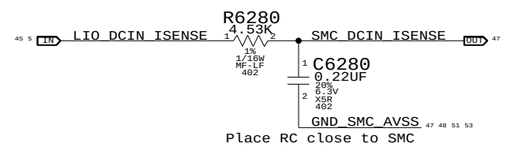
PBUS Voltage Sense Enable & Filter



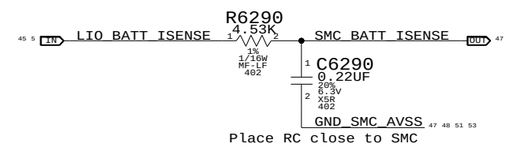
FireWire Current Sense Filter



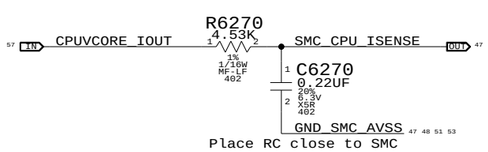
DCIN Current Sense Filter



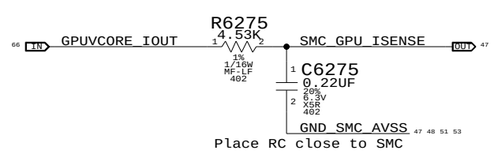
Battery Current Sense Filter



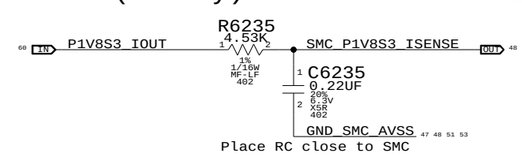
CPU Current Sense Filter



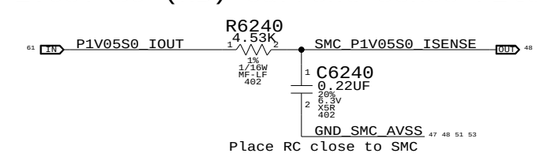
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

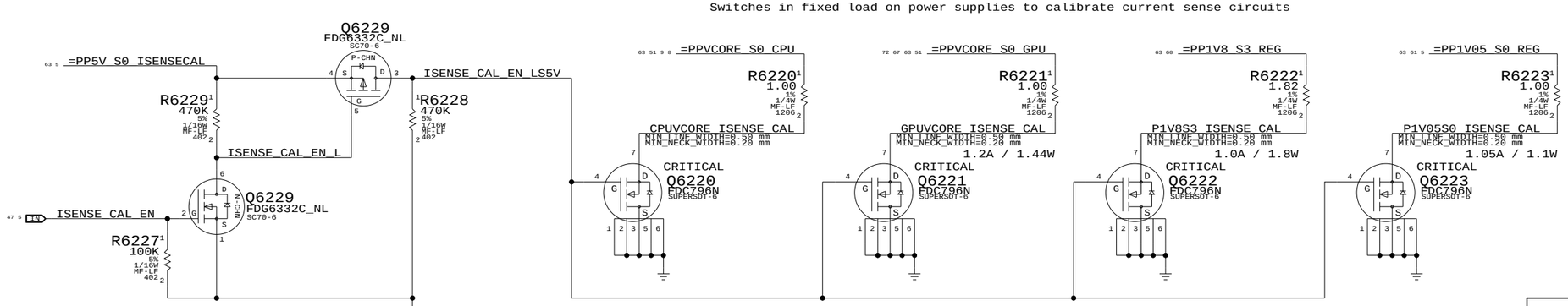


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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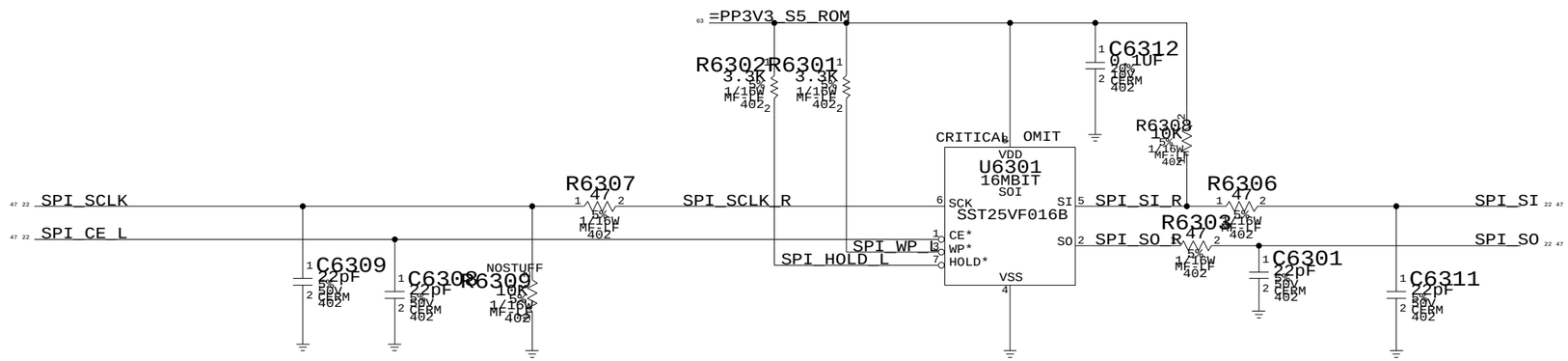
SCALE NONE	SHT 62 OF 104	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=MSZ SYNC_DATE=11/16/2005

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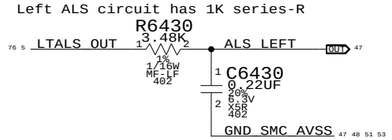
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

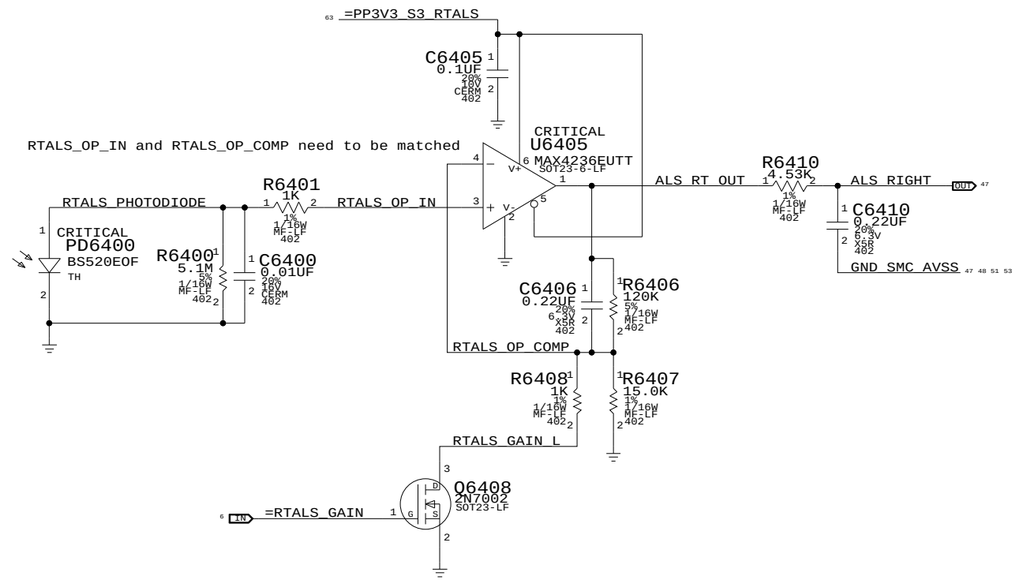
SCALE	SHT	OF
NONE	63	104

Left ALS Filter

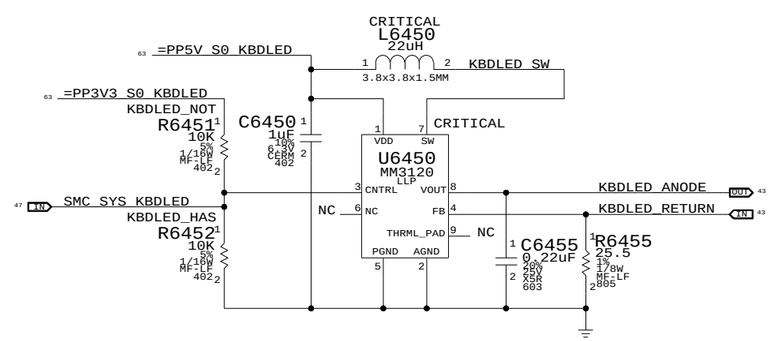
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



ALS Support	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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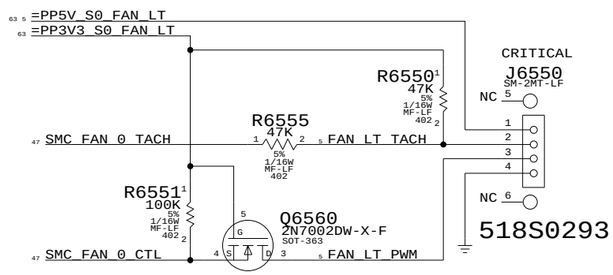
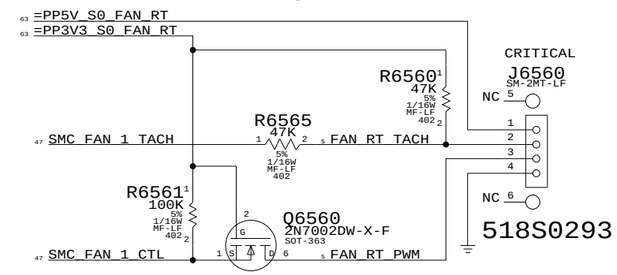
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 64 OF 104	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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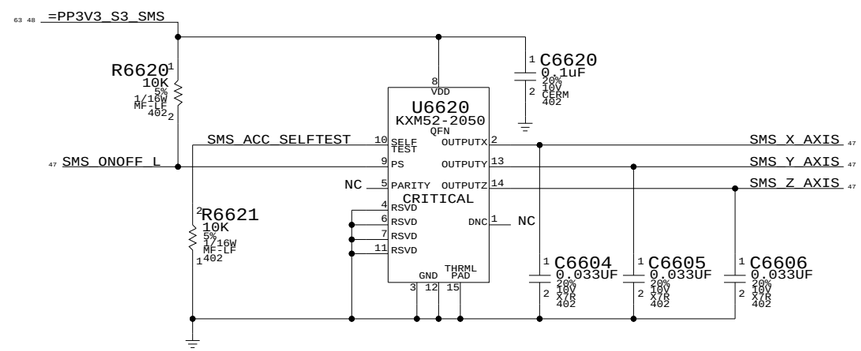
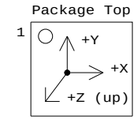
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	65	104



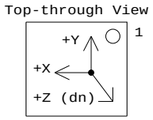
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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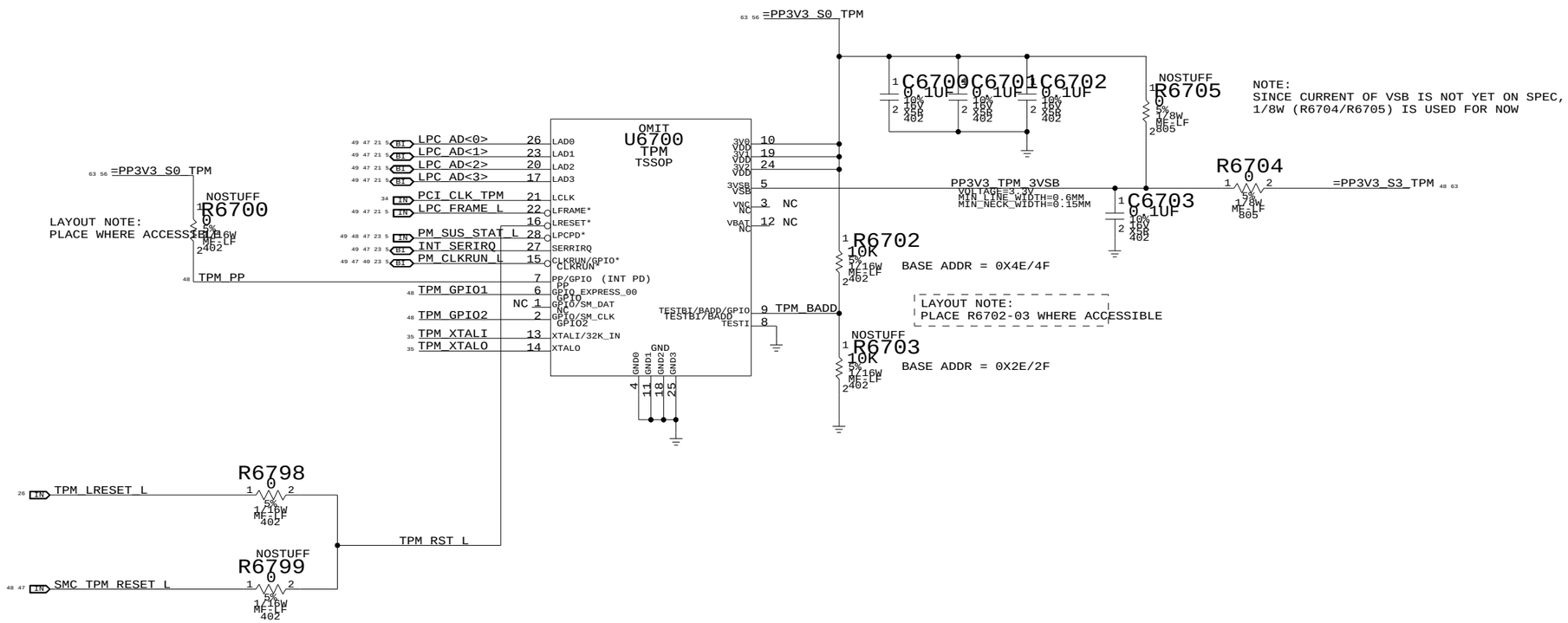
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE

SHT 66 OF 104



TPM

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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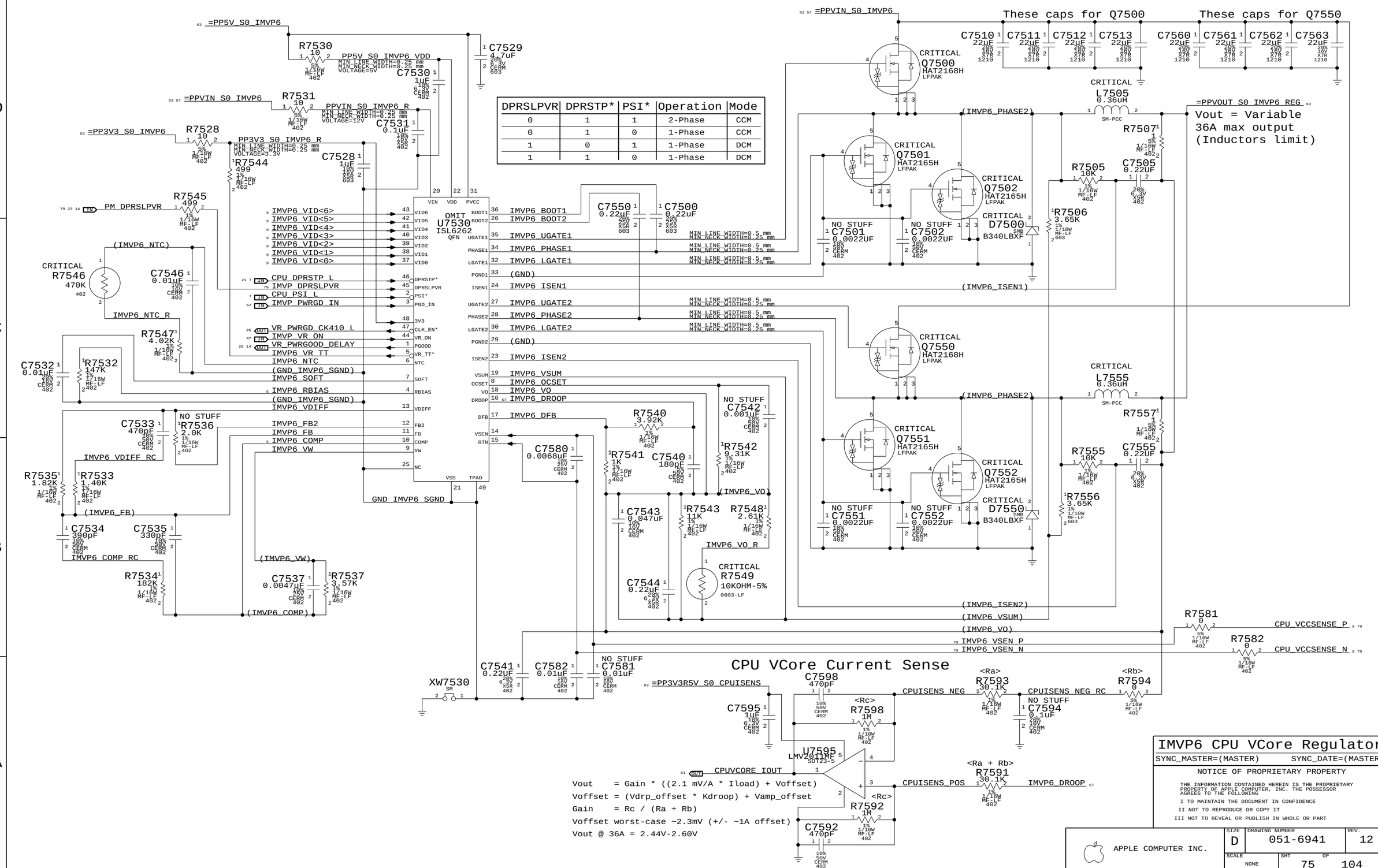
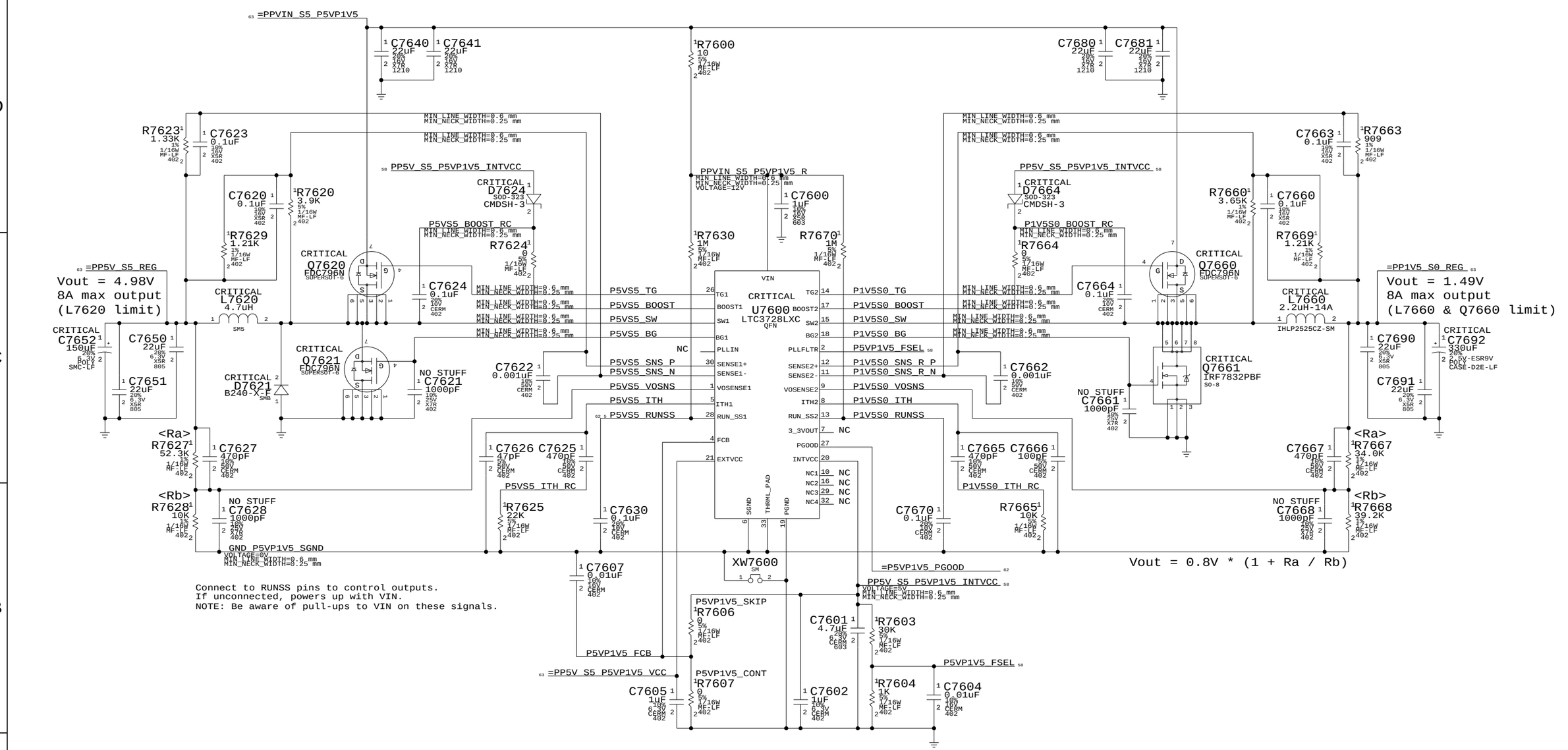
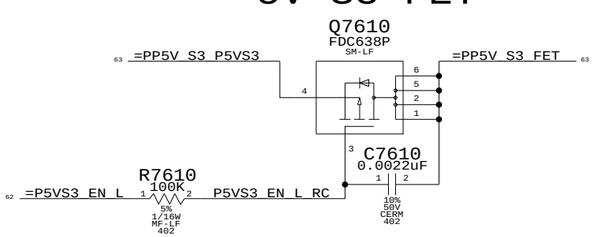
SCALE NONE	SHT 67 OF 104	



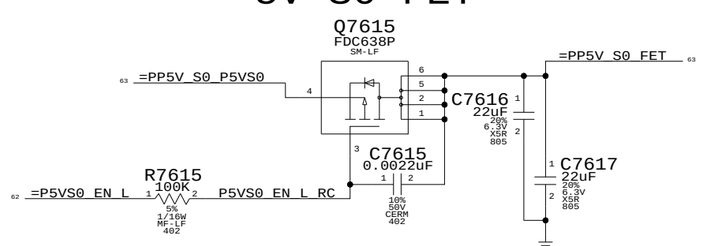
DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM



5V S3 FET



5V S0 FET



5V / 1.5V Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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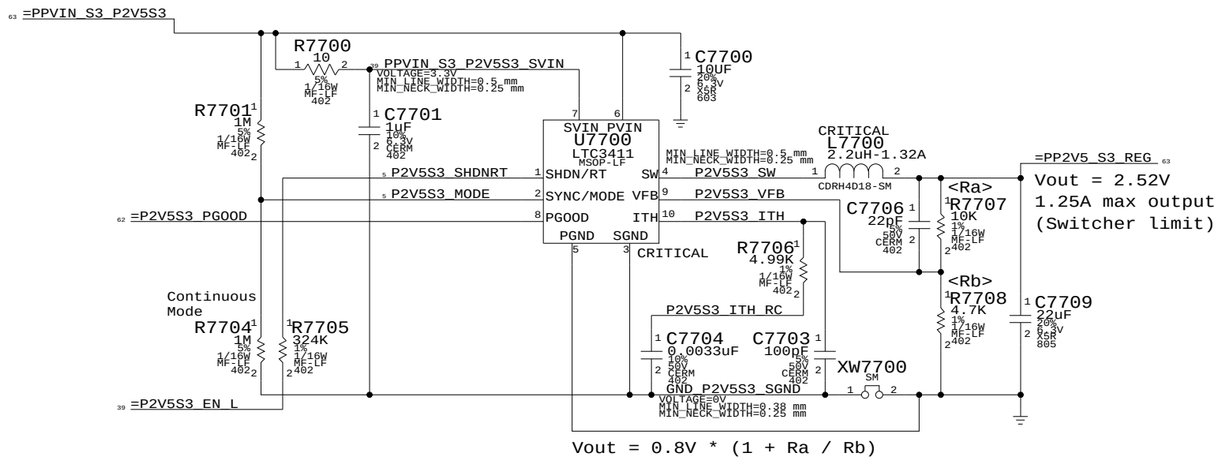
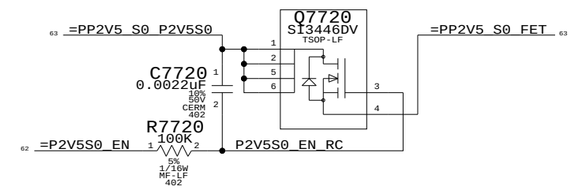
SCALE: NONE SHT 76 OF 104

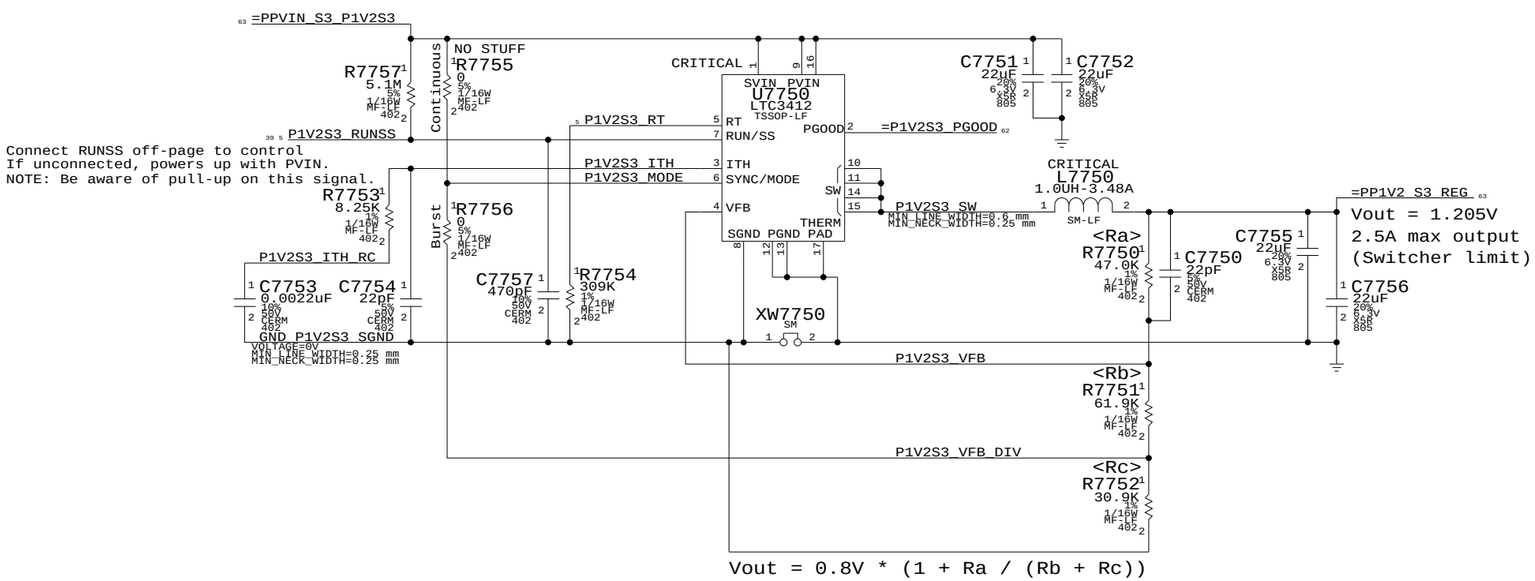
2.5V S3 Regulator



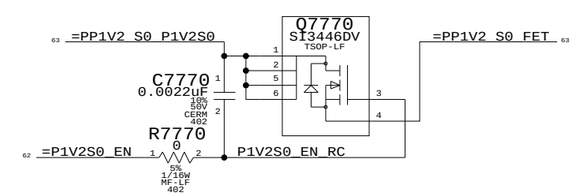
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

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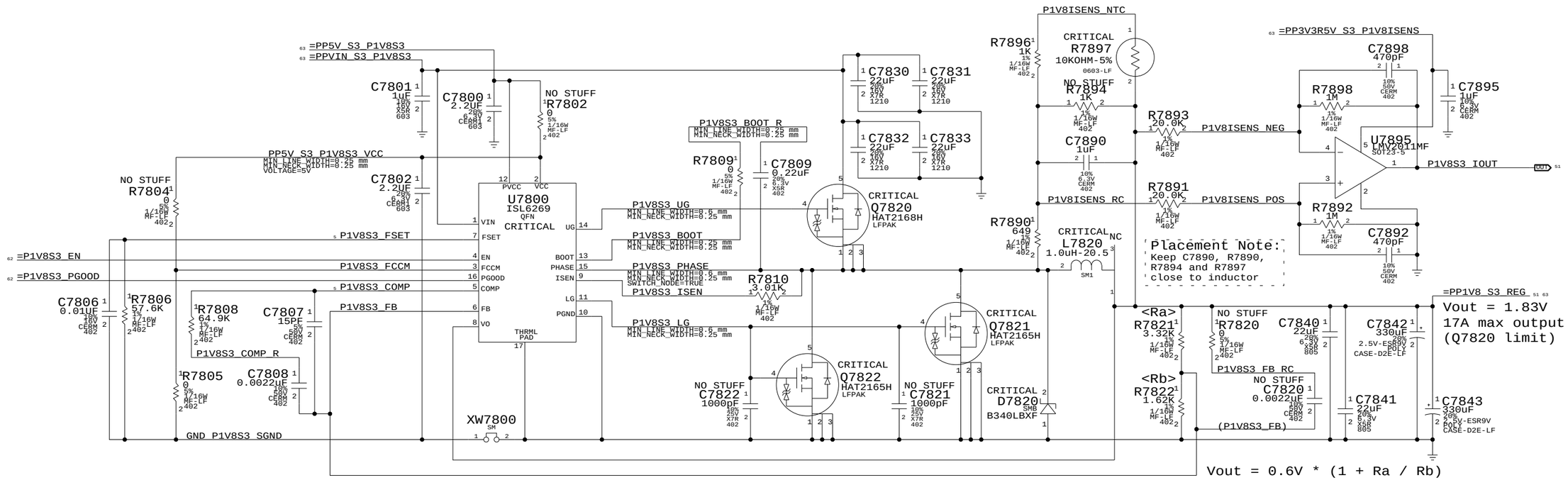
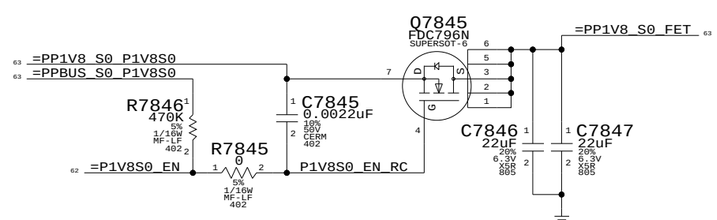
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 77	OF 104

1.8V S3 Current Sense



1.8V S0 FET



1.8V Supply

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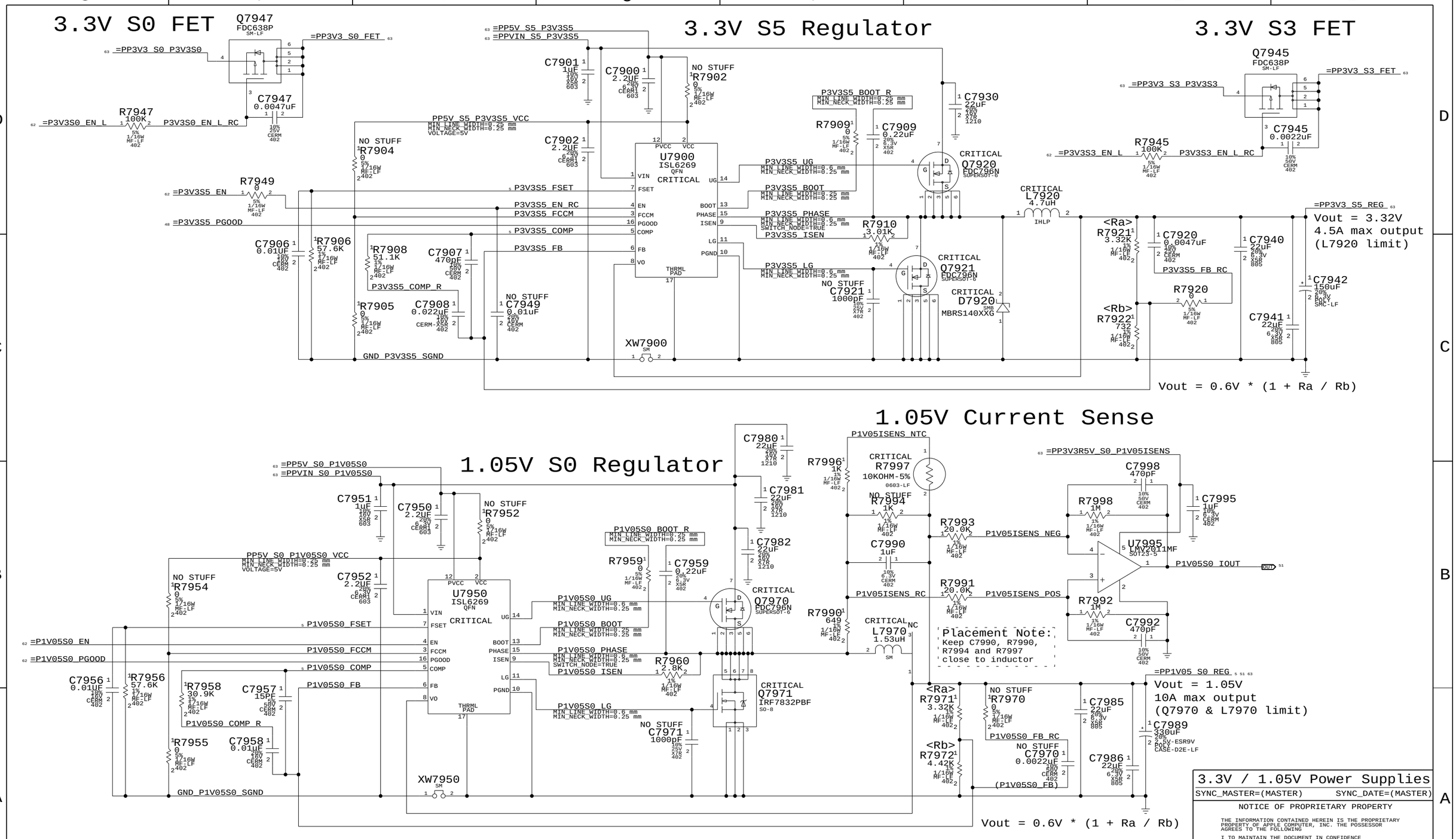
D	051-6941	12
SCALE NONE	SHT 78 OF 104	



3.3V / 1.05V Power Supplies

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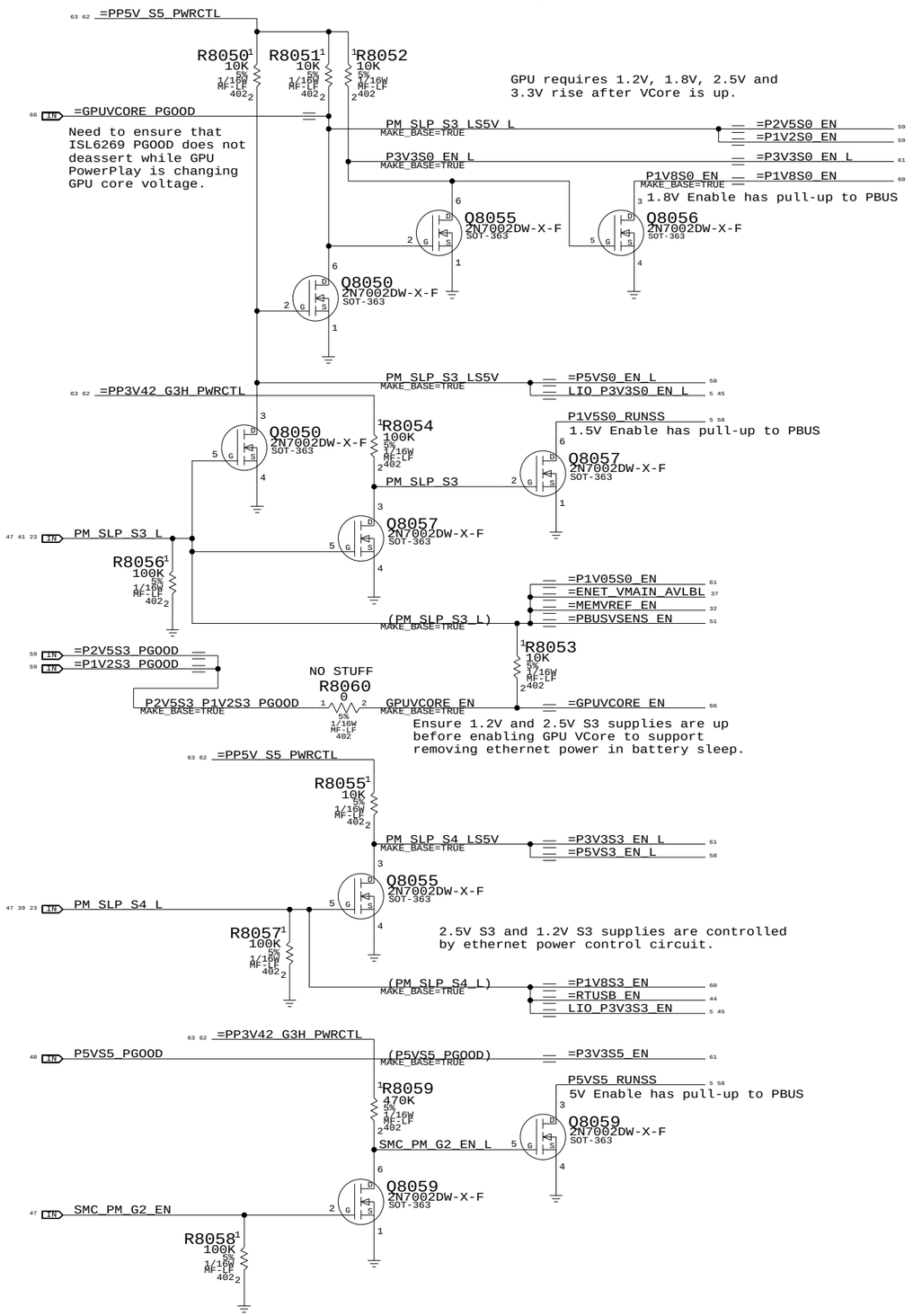
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE NONE | SHT 79 OF 104

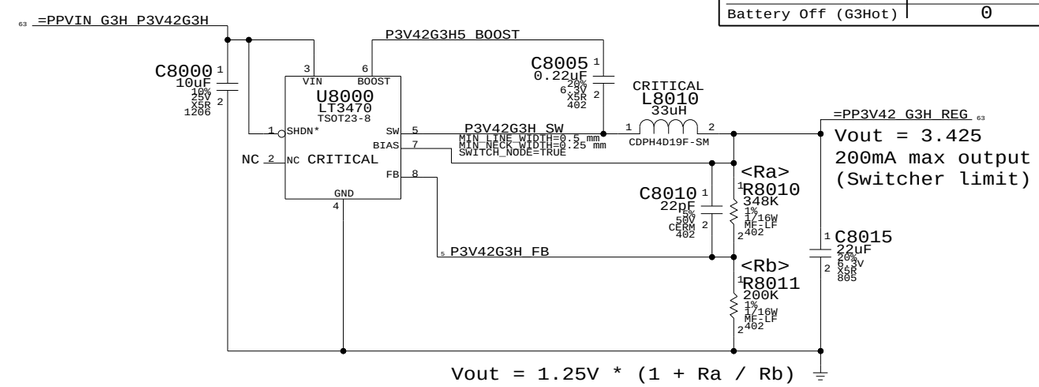
Power Control Signals



3.425V "G3Hot" Supply

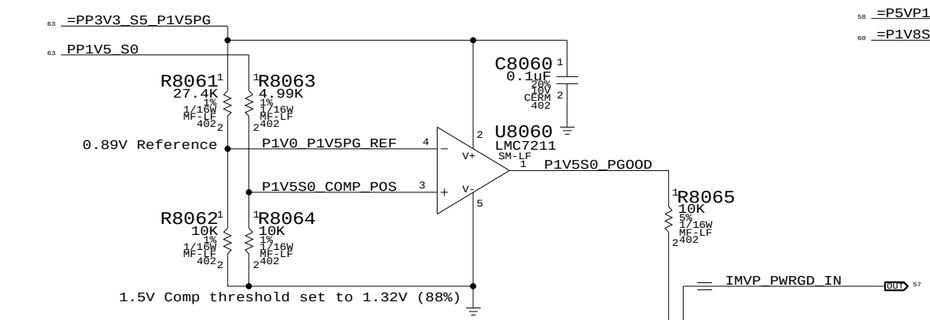
Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



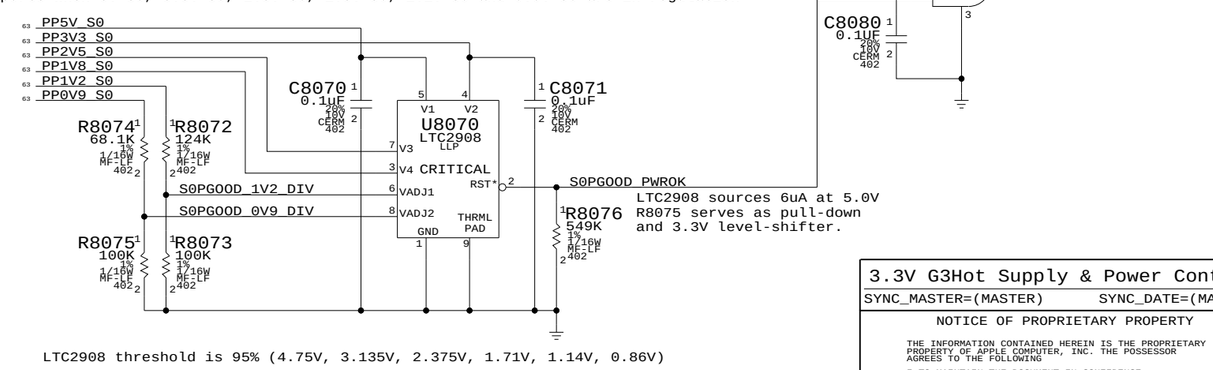
Unused PGOOD Signals

=P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

=P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



3.3V G3Hot Supply & Power Control

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SCALE NONE — SHT 80 OF 104

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

=PP0V9 S0 MEMVTT LDO → PP0V9 S0 (MIN LINE WIDTH=0.38 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=0.9V, MAKE BASE=TRUE) → =PP0V9 S0 MEM TERM

=PP1V05 S0 REG → PP1V05 S0 (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.05V, MAKE BASE=TRUE)
- =PP1V05 S0 CPU
- =PP1V05 S0 FSB NB
- =PP1V05 S0 NB CRT
- =PP1V05 S0 NB VTT
- =PP1V05 S0 SB CPU IO
- =PP1V05 S0 PHYSSEC
- =PPVCORE S0 NB
- =PPVCORE S0 SB

=PP1V2 S3 REG → PP1V2 S3 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.22 mm, VOLTAGE=1.2V, MAKE BASE=TRUE)
- =PP1V2 S3 ENET
- =PP1V2 S0 P1V2S0

=PP1V2 S0 FET → PP1V2 S0 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.2V, MAKE BASE=TRUE)
- =PP1V2 S0 GPU VDDPLL
- =PP1V2 S0 PCIE GPU
- =PP1V2 S0 PCIE GPU PVDD
- =PP1V2 S0 PCIE GPU VDDR

PP1V5 S0 REG (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.4 mm, VOLTAGE=1.5V, MAKE BASE=TRUE) → =PP1V5 S0 REG → XW8115 (JUMPER OPEN)
PLACEMENT_NOTE=Place on top-side of board

=PP1V5 S0 REG → PP1V5 S0 (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.5V, MAKE BASE=TRUE)
- =PP1V5 S0 CPU
- =PP1V5 S0 NB
- =PP1V5 S0 NB 3G
- =PP1V5 S0 NB 3GPLL
- =PP1V5 S0 NB PCIE
- =PP1V5 S0 NB PLL
- =PP1V5 S0 NB TVDAC
- =PP1V5 S0 NB VCCAUX
- =PP1V5 S0 NB VCCD_HMPLL
- =PP1V5 S0 SB
- =PP1V5 S0 SB VCC1_5_A
- =PP1V5 S0 SB VCC1_5_A_ARX
- =PP1V5 S0 SB VCC1_5_A_ATX
- =PP1V5 S0 SB VCC1_5_A_USB_CORE
- =PP1V5 S0 SB VCCSATAPLL
- =PP1V5 S0 SB VCCUSBPLL
- =PP1V5 S0 LIO

PP1V8 S3 REG (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE BASE=TRUE) → =PP1V8 S3 REG → XW8118 (JUMPER OPEN)
PLACEMENT_NOTE=Place on top-side of board

=PP1V8 S3 REG → PP1V8 S3 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE BASE=TRUE)
- =PP1V8 S3 MEM
- =PP1V8 S3 MEM_NB
- =PP1V8 S3 MEMVREF
- =PP1V8 S0 MEMVTT
- =PP1V8 S0 P1V8S0

PP1V8 S0 FET (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE BASE=TRUE) → =PP1V8 S0 FET → XW8119 (JUMPER OPEN)
PLACEMENT_NOTE=Place on top-side of board

=PP1V8 S0 FET → PP1V8 S0 GPU (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE BASE=TRUE)
- =PP1V8R2V0 S0 FB GPU
- =PP1V8 S0 FB VDD
- =PP1V8 S0 FB VDDQ

PP2V5 S3 REG (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.3 mm, VOLTAGE=2.5V, MAKE BASE=TRUE) → =PP2V5 S3 REG → XW8125 (JUMPER OPEN)
PLACEMENT_NOTE=Place on top-side of board

=PP2V5 S3 REG → PP2V5 S3 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=2.5V, MAKE BASE=TRUE)
- =PP2V5 S3 ENET
- =PP2V5 S0 P2V5S0

=PP2V5 S0 FET → PP2V5 S0 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=5V, MAKE BASE=TRUE)
- =PP2V5 S0 NB VCCA 3GBG
- =PP2V5 S0 GPU
- =PP2V5 S0 GPU PVDD
- =PP2V5 S0 GPU VDD25
- =PP2V5 S0 GPU VDDC_CT

=PPVCORE S0 GPU REG → PPVCORE S0 GPU (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.2V, MAKE BASE=TRUE)
- =PPVCORE S0 GPU
- =PPVCORE S0 GPU BBP

=PPDCIN G3H LIO → PPDCIN G3H (MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=18.5V, MAKE BASE=TRUE) → =PPVIN G3H P3V42G3H

GND (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=0V)

=PP3V42 G3H REG → PP3V42 G3H (MIN LINE WIDTH=0.25 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.42V, MAKE BASE=TRUE)
- =PP3V42 G3H SMCVREF
- =PP3V42 G3H SMBUS SMC BSA
- =PP3V42 G3H PWRCTL
- =PP3V42 G3H SB RTC
- =PP3V42 G3H SMC PWRGD
- =PP3V42 G3H SMC CLK
- =PP3V42 G3H LIO
- =PP3V42 G3H PBUSVSENS
- =PP3V42 G3H LIDSWITCH
- =PP3V3 S5 SMC
- =PP3V3 S5 LPCPLUS

PP3V3 S5 REG (MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE BASE=TRUE) → =PP3V3 S5 REG → XW8133 (JUMPER OPEN)
PLACEMENT_NOTE=Place on top-side of board

=PP3V3 S5 REG → PP3V3 S5 (MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE BASE=TRUE)
- =PP3V3 S5 SB
- =PP3V3 S5 SB 3V3 1V5 VCCSUSHDA
- =PP3V3 S5 SB IO
- =PP3V3 S5 SB PM
- =PP3V3 S5 SB USB
- =PP3V3 S5 SB VCCSUS3 3
- =PP3V3 S5 SB VCCSUS3 3 USB
- =PP3V3 S5 ROM
- =PP3V3 S5 P1V5PG
- =PP3V3 S5 FWLATEVG
- =PP3V3 S3 P3V3S3
- =PPVIN S3 P2V5S3
- =PP3V3 S0 LCD
- =PP3V3 S0 P3V3S0

=PP3V3 S3 FET → PP3V3 S3 (MIN LINE WIDTH=0.5 MM, MIN NECK WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE BASE=TRUE)
- =PP3V3 S3 P3V3S3AC
- =PP3V3 S3 RTALS
- =PP3V3 S3 SMBUS SMC A S3
- =PP3V3 S3 TPM
- =PP3V3 S3 SMS
- =PP3V3 S3 BT
- =PP3V3 S3 TOPCASE
- =PP3V3 S3 LTALS
- =PP3V3 S3 MEMVREF
- =PP3V3 S3 FW
- =PP3V3 S3 PCI
- =PP3V3R5V S3 P1V8ISENS
- =PPVIN S3 P1V2S3

=PP3V3 S0 FET → PP3V3 S0 (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE BASE=TRUE)
- =PP3V3 S0 DDC DVI
- =PP3V3 S0 DDC LCD
- =PP3V3 S0 CK410
- =PP3V3 S0 IDE
- =PP3V3 S0 IMVP6
- =PP3V3 S0 INVERTER
- =PP3V3 S0 NB
- =PP3V3 S0 NB VCC HV
- =PP3V3 S0 SB
- =PP3V3 S0 SB 3V3 1V5 VCCHDA
- =PP3V3 S0 SB GPIO
- =PP3V3 S0 SB PCI
- =PP3V3 S0 SB PM
- =PP3V3 S0 SB VCC3 3
- =PP3V3 S0 SB VCC3 3 IDE
- =PP3V3 S0 SB VCC3 3 PCI
- =PP3V3 S0 SB VCCLAN3 3
- =PP3V3 S0 TPM
- =PP3V3 S0 VGASYNC
- =PP3V3 S0 KBDLED
- =PP3V3 S0 THRM SNR
- =PP3V3 S0 GPUTHMSNS
- =PP3V3 S0 RSTHMSNS
- =PP3V3 S0 SMBUS SB
- =PP3V3 S0 SMBUS SMC 0 S0
- =PP3V3 S0 SMBUS SMC B S0
- =PP3V3 S0 SMBUS SMC BSB
- =PP3V3 S0 RSTBUF
- =PP3V3 S0 SMC LS
- =PP3V3 S0 ALLSYSPG
- =PP3V3 S0 FAN LT
- =PP3V3 S0 FAN RT
- =PP3V3 S0 FWISENS
- =PP3V3R5V S0 CPUISENS
- =PP3V3R5V S0 GPUISENS
- =PP3V3R5V S0 P1V05ISENS
- =PP3V3R5V S0 P1V8ISENS
- =PPSPD S0 MEM

R8133 0 5% 1/8W MF-LF 805
PLACEMENT_NOTE=Place on top-side of board

PP3V3 S0 GPU (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE BASE=TRUE)
- =PP3V3 S0 GPU
- =PP3V3 S0 GPUBBP
- =PP3V3 S0 GPUBBN
- =PP3V3 S0 GPU VDDR3
- =PP3V3 S0 GPU GPIOS
- =PP1V8R3V3 S0 GPU VDDR4
- =PP1V8R3V3 S0 GPU VDDR5

=PP3V3 S3AC FET → PP3V3 S3AC (MIN LINE WIDTH=0.38 mm, MIN NECK WIDTH=0.22 mm, VOLTAGE=3.3V, MAKE BASE=TRUE)
- =PP3V3 S3 ENET

=PNVOUT S0 GPUBBN REG → PNBB S0 GPU (MIN LINE WIDTH=0.25 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=0.7V, MAKE BASE=TRUE)
- =PNBB S0 GPU

=PPVOUT S0 GPUBBP LDO → PPBB S0 GPU (MIN LINE WIDTH=0.25 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=1.8V, MAKE BASE=TRUE)
- =PPBB S0 GPU

=PPVOUT S0 IMVP6 REG → PPVCORE S0 CPU (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=1.2V, MAKE BASE=TRUE)
- =PPVCORE S0 CPU

=PPBUS G3H LIO CONN → PPBUS G3H (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=12.6V, MAKE BASE=TRUE)
- =PPBUS G3H S3AC
- =PPVIN S5 P5VP1V5
- =PPVIN S0 IMVP6
- =PPVIN S5 P3V3S5
- =PPBUS S5 FWPWRSW
- =PPVIN S3 P1V8S3
- =PPVIN S0 P1V05S0
- =PPVIN S0 GPUVCORE
- =PPBUS S0 INVERTER
- =PPBUS S0 P1V8S0

=PPBUS S5 FW FET → PPBUS S5 FW FET (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.3 mm, VOLTAGE=3.3V, MAKE BASE=TRUE)
- =PPFW PORT1

=PP5V S5 REG (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.3 mm, VOLTAGE=5V, MAKE BASE=TRUE) → =PP5V S5 REG → XW8150 (JUMPER OPEN)
PLACEMENT_NOTE=Place on top-side of board

=PP5V S5 REG → PP5V S5 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=5V, MAKE BASE=TRUE)
- =PP5V S5 SB
- =PP5V S5 P3V3S5
- =PP5V S5 P5VP1V5 VCC
- =PP5V S5 LIO
- =PP5V S5 PWRCTL
- =PP5V S3 P5VS3
- =PP5V S3 P1V8S3
- =PP5V S3 RTUSB
- =PP5V S0 P5VS0
- =PP5V S0 GPUVCORE
- =PP5V S0 P1V05S0

=PP5V S3 FET → PP5V S3 (MIN LINE WIDTH=0.5 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=5V, MAKE BASE=TRUE)
- =PP5V S3 SYSLED
- =PP5V S3 CAMERA
- =PP5V S3 IR
- =PP5V S3 TOPCASE

=PP5V S0 FET → PP5V S0 (MIN LINE WIDTH=0.6 mm, MIN NECK WIDTH=0.25 mm, VOLTAGE=5V, MAKE BASE=TRUE)
- =PP5V S0 DVI DDC
- =PP5V S0 IDE
- =PP5V S0 HDD
- =PP5V S0 IMVP6
- =PP5V S0 INVERTER
- =PP5V S0 MEMVTT
- =PP5V S0 SB
- =PP5V S0 FAN LT
- =PP5V S0 FAN RT
- =PP5V S0 KBDLED
- =PP5V S0 GPUBBCTL
- =PP5V S0 LPCPLUS
- =PP5V S0 AUDIO XW
- =PP5V S0 ISENSECAL

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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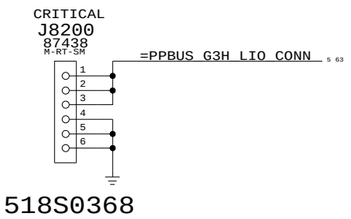
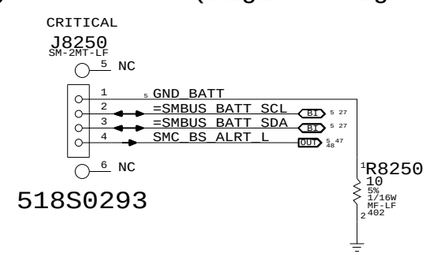
Left I/O Power Connector



Battery Connector (Digital Signals)



PBus-In & Battery Connectors			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		

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D	051-6941	12
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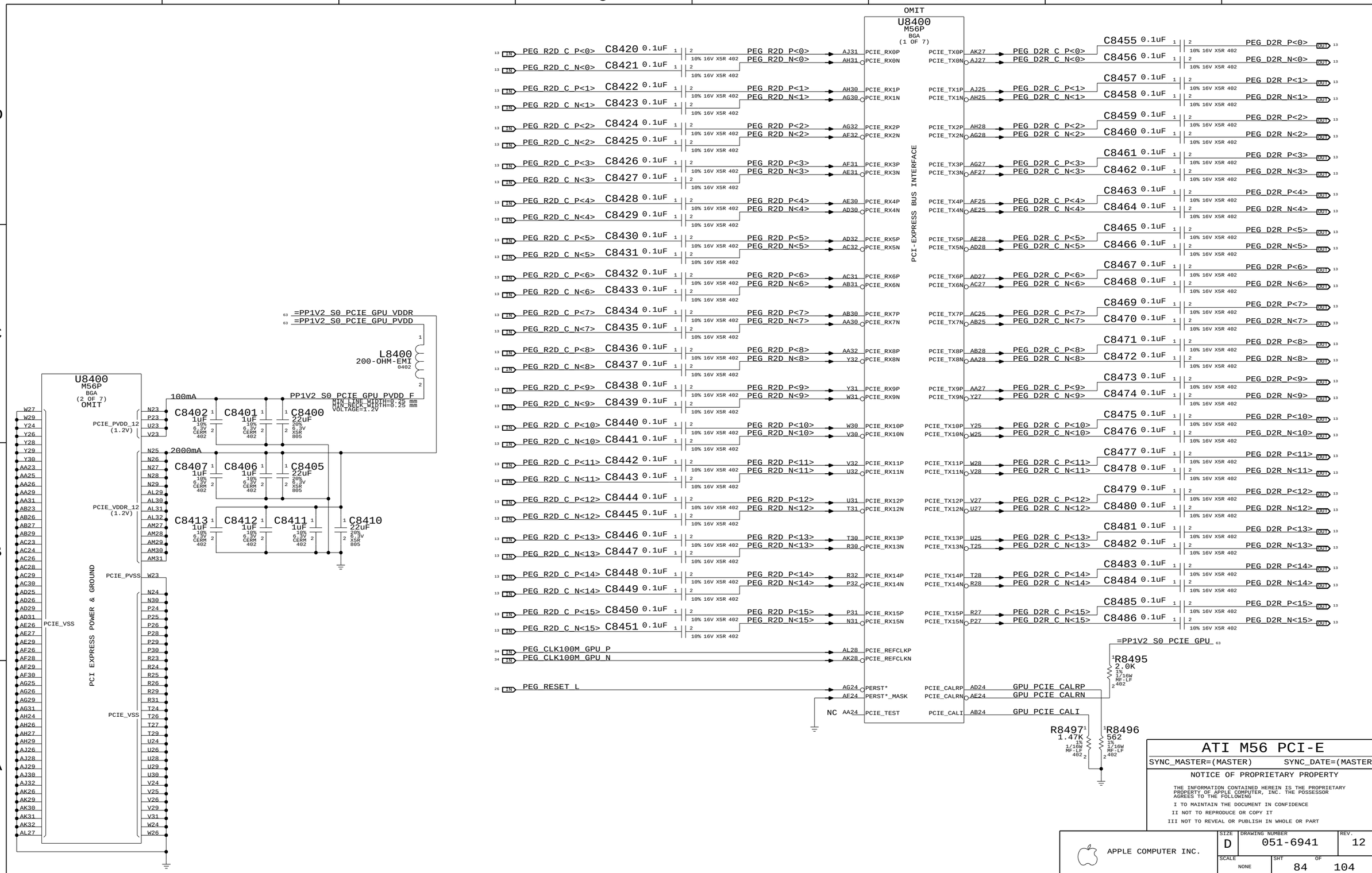
OMIT
U8400
M56P
BGA
(1 OF 7)
PCI-EXPRESS BUS INTERFACE
PCI EXPRESS POWER & GROUND
=PP1V2_S0_PCIE_GPU_VDDR
=PP1V2_S0_PCIE_GPU_PVDD
L8400
200-OHM-EMI
PP1V2_S0_PCIE_GPU_PVDD_F
100mA
2000mA
PCIE_PVDD_12 (1.2V)
PCIE_VDDR_12 (1.2V)
PCIE_PVSS
PCIE_VSS
PEG_CLK100M_GPU_P
PEG_CLK100M_GPU_N
PEG_RESET_L
=PP1V2_S0_PCIE_GPU
R8495 2.0K
R8497 1.47K
R8496 562
GPU_PCIE_CALRP
GPU_PCIE_CALRN
GPU_PCIE_CALI
NC
ATI M56 PCI-E
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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SIZE D
DRAWING NUMBER 051-6941
REV. 12
SCALE NONE
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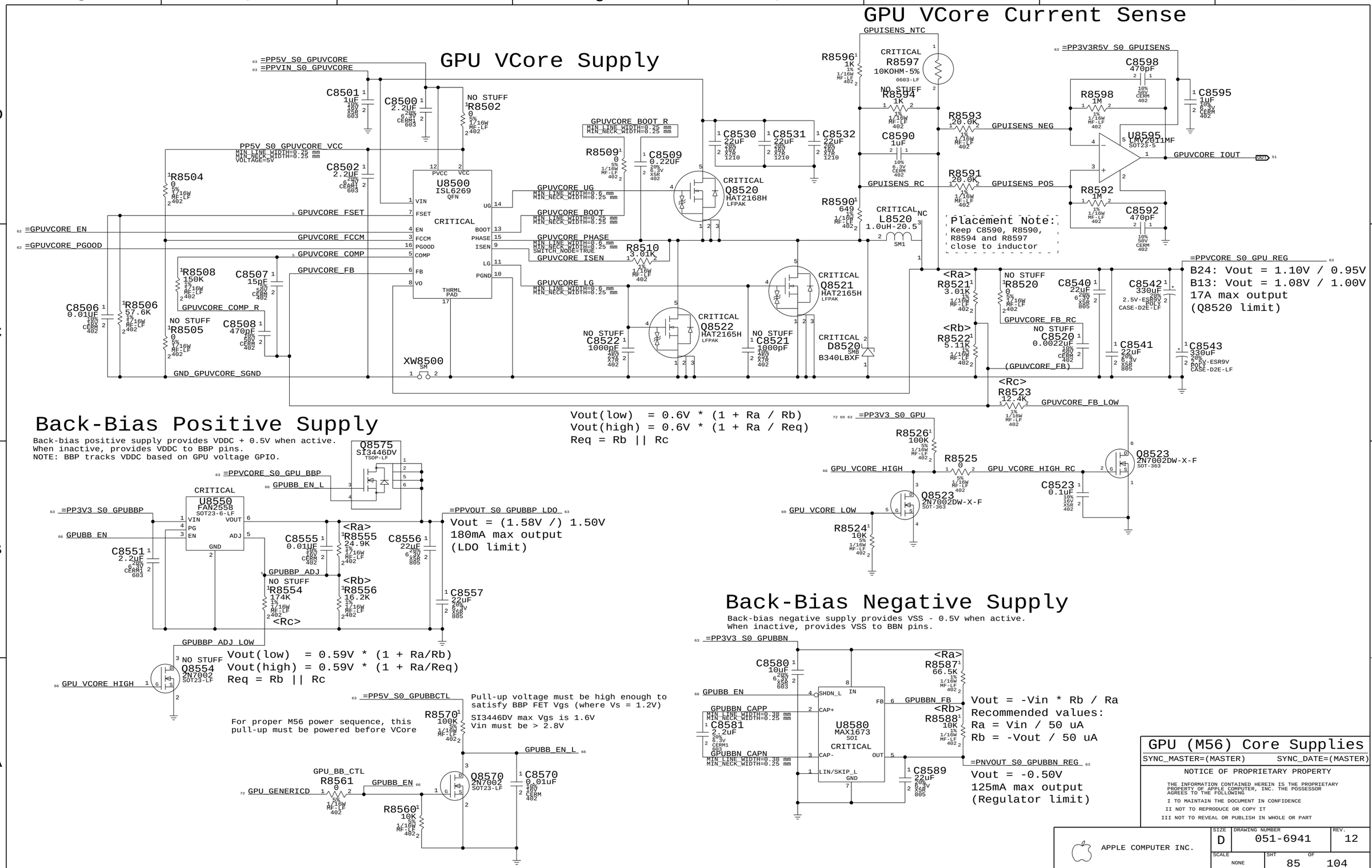
GPU VCore Current Sense



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	12
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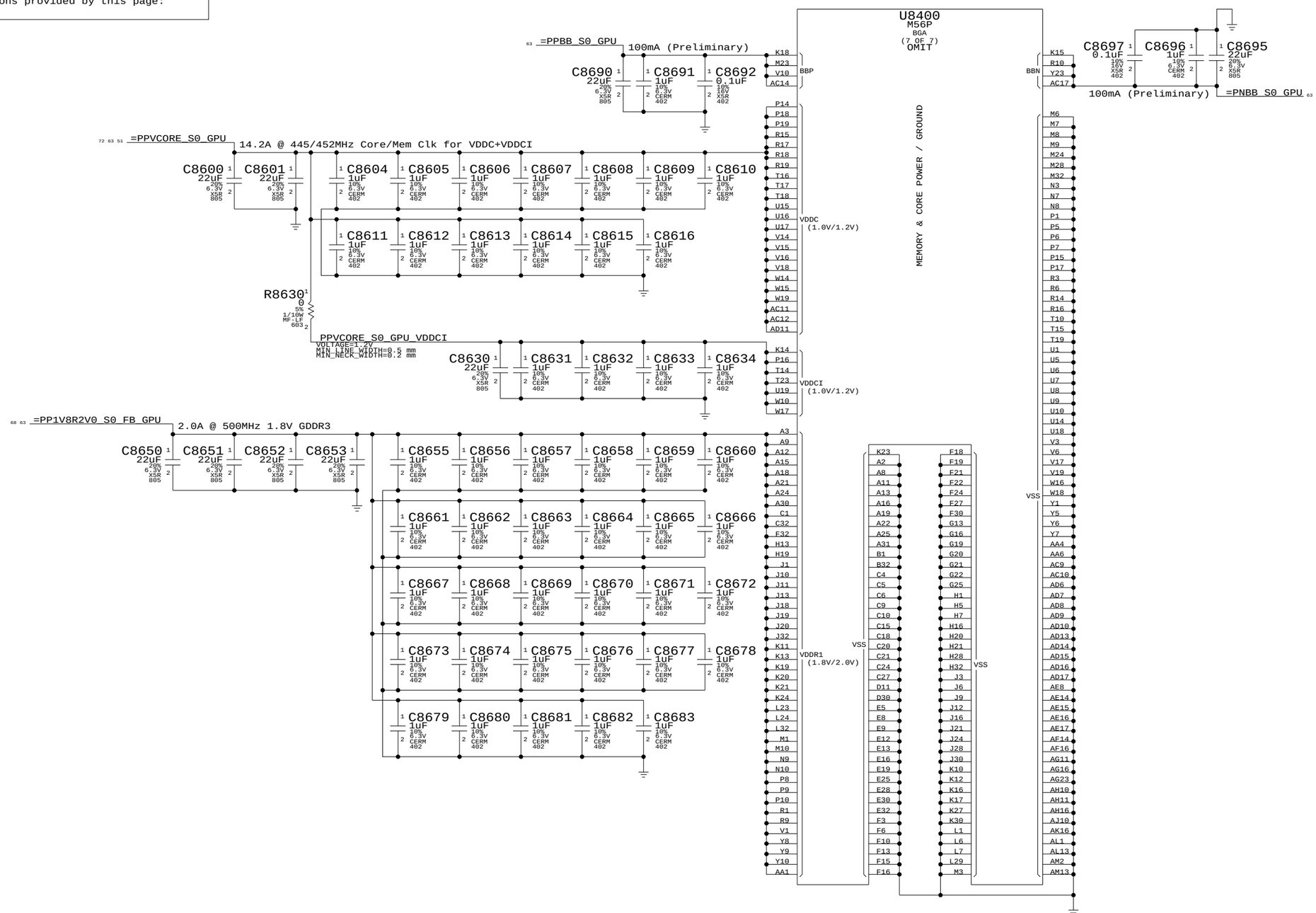
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

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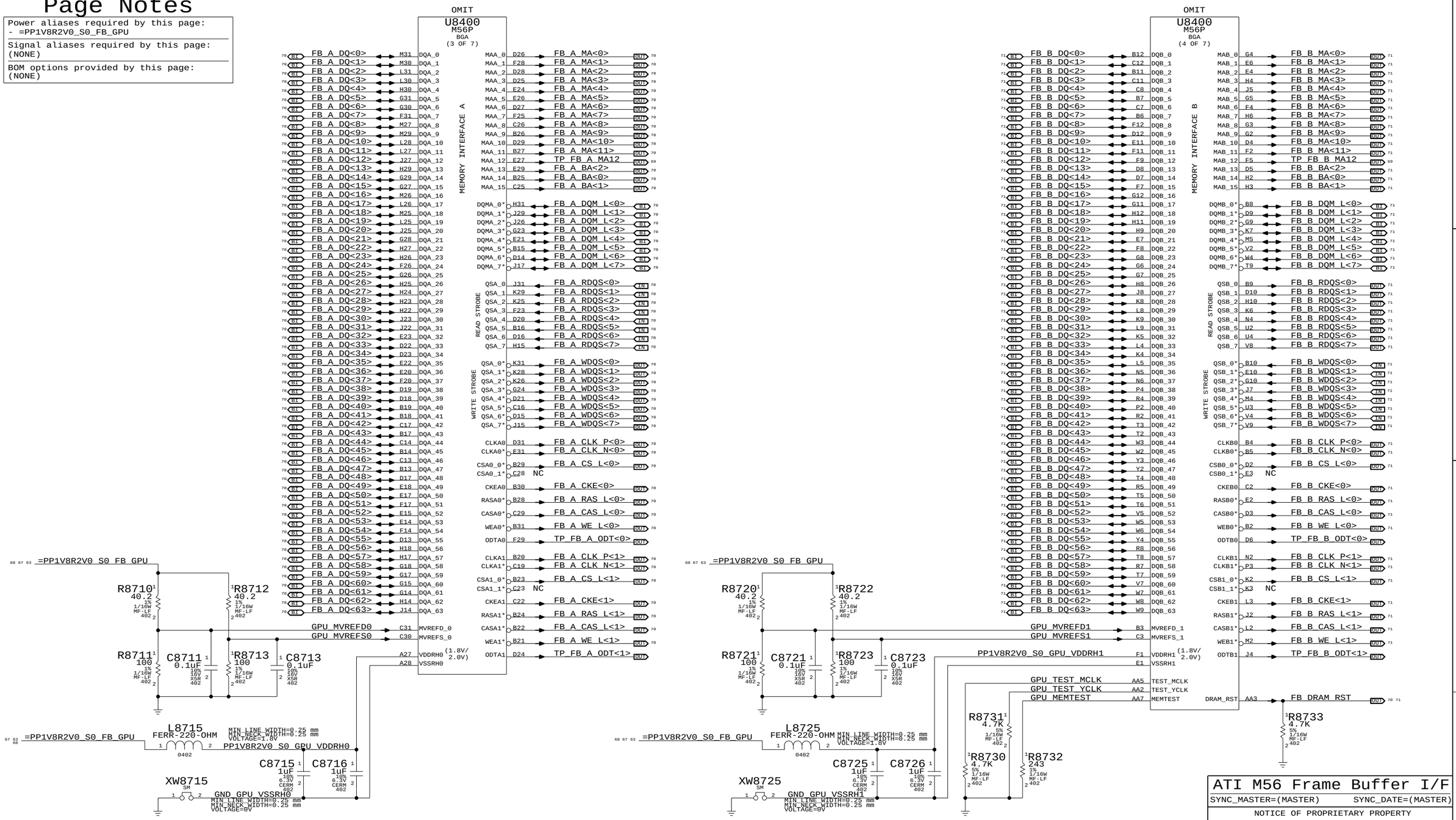
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

63 =PP3V3_S0_GPU_GPIOS

R8800[1] 10K 5% 1/16W MF-LF 402						
NO STUFF R8802[1] 10K 5% 1/16W MF-LF 402						
NO STUFF R8804[1] 10K 5% 1/16W MF-LF 402						
NO STUFF R8806[1] 10K 5% 1/16W MF-LF 402						
NO STUFF R8809[1] 10K 5% 1/16W MF-LF 402						
GPU_MEM_256M R8812[1] 10K 5% 1/16W MF-LF 402						
GPU_MEM_256M R8824[1] 10K 5% 1/16W MF-LF 402						
	GPU_DEEPMH_EN R8801[1] 10K 5% 1/16W MF-LF 402					
		NO STUFF R8803[1] 10K 5% 1/16W MF-LF 402				
			R8805[1] 10K 5% 1/16W MF-LF 402			
				NO STUFF R8808[1] 10K 5% 1/16W MF-LF 402		
					GPU_MEM_64M R8813[1] 10K 5% 1/16W MF-LF 402	
						NO STUFF R8811[1] 10K 5% 1/16W MF-LF 402
						GPU_MEM_HYNIX R8827[1] 10K 5% 1/16W MF-LF 402

	Serial ROM	TestBus	Misc	Straps		
72 GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb		
72 GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN		
72 GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved		
72 GPU_GPIO_3		TESTIN[3]		Reserved		
72 GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS		
72 GPU_GPIO_5		TESTIN[5]		Reserved		
72 GPU_GPIO_6		TESTIN[6]		Reserved		
72 GPU_GPIO_7	ENA_BL	TESTIN[7]			GPU_BLON (MAKE_BASE=TRUE) 74	
72 GPU_GPIO_8	ROMSO	TESTWR		Reserved		
72 GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]		
72 GPU_GPIO_10	ROMSCK	TESTOUT[8]			TP_GPU_GPIO_10 (MAKE_BASE=TRUE)	Required for debug access
72 GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]		Required for debug access
72 GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]		Required for debug access
72 GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]		Required for debug access
72 GPU_GPIO_14		TESTIN[8]			NC_GPU_GPIO_14 (MAKE_BASE=TRUE) NO_TEST=TRUE	
72 GPU_GPIO_15		TESTIN[9]	PWRCNTL		GPU_VCORE_LOW (MAKE_BASE=TRUE) 66	
72 GPU_GPIO_16			SS_IN		GPU_CLK27MSS_IN (MAKE_BASE=TRUE) 34	
72 GPU_GPIO_17			Thm Mon Int		NC_GPU_GPIO_17 (MAKE_BASE=TRUE) NO_TEST=TRUE	
72 GPU_GPIO_18				NC_GPU_GPIO_18 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_19				NC_GPU_GPIO_19 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_20				NC_GPU_GPIO_20 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_21				NC_GPU_GPIO_21 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_22				NC_GPU_GPIO_22 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_23				NC_GPU_GPIO_23 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_24					GPU_MEM_256M (MAKE_BASE=TRUE)	
72 GPU_GPIO_25				NC_GPU_GPIO_25 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_26				NC_GPU_GPIO_26 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_27					GPU_MEMID (MAKE_BASE=TRUE)	
72 GPU_GPIO_28				NC_GPU_GPIO_28 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_29				NC_GPU_GPIO_29 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_30				NC_GPU_GPIO_30 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_31				NC_GPU_GPIO_31 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_32				NC_GPU_GPIO_32 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_33				NC_GPU_GPIO_33 (MAKE_BASE=TRUE NO_TEST=TRUE)		
72 GPU_GPIO_34				NC_GPU_GPIO_34 (MAKE_BASE=TRUE NO_TEST=TRUE)		

Renamed signals

34 GPU_CLK27M (MAKE_BASE=TRUE)		GPU_XTALIN 72

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_XTALOUT 72
NC_ATI_ROMCS_L (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_ATI_ROMCS_L 72
NC_FB_A_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_A_MA12 68
NC_FB_B_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_B_MA12 68
NC_GPU_GENERICA (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICA 72
NC_GPU_GENERICB (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICB 72
NC_GPU_GENERICC (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICC 72
NC_GPU_VGA_R (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_R 73
NC_GPU_VGA_G (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_G 73
NC_GPU_VGA_B (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_B 73
TP_GPU_VGA_HSYNC (MAKE_BASE=TRUE)		GPU_VGA_HSYNC 73
TP_GPU_VGA_VSYNC (MAKE_BASE=TRUE)		GPU_VGA_VSYNC 73
NC_GPU_TV_Y (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_Y 73
NC_GPU_TV_C (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_C 73
NC_GPU_TV_COMP (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_COMP 73
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_P<3> 73
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_N<3> 73
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_P<3> 73
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_N<3> 73
NC_ATI_DVPCLK (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCLK 72
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCNTL<2..0> 72
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPDATA<15..0> 72

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) — ATI_DVPDATA<23..16> 72

Also required: GPIO10 - GPIO13

72 66 63 =PP3V3_S0_GPU

R9390[1] 4.7K 5% 1/16W MF-LF 402	R9391[1] 4.7K 5% 1/16W MF-LF 402

73 GPU_DDC_B_CLK
73 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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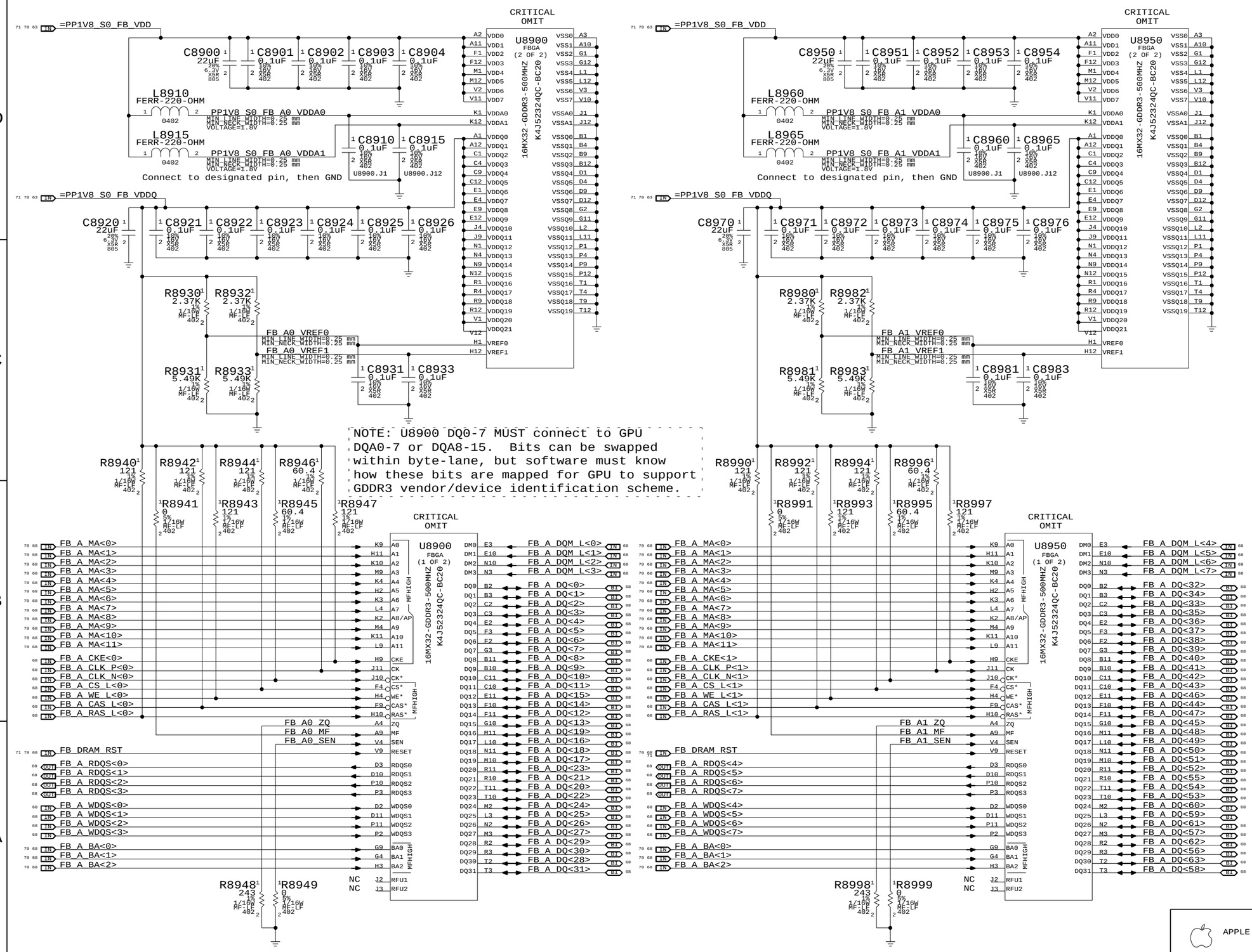
D	051-6941	12

SCALE NONE — SHT 88 OF 104



NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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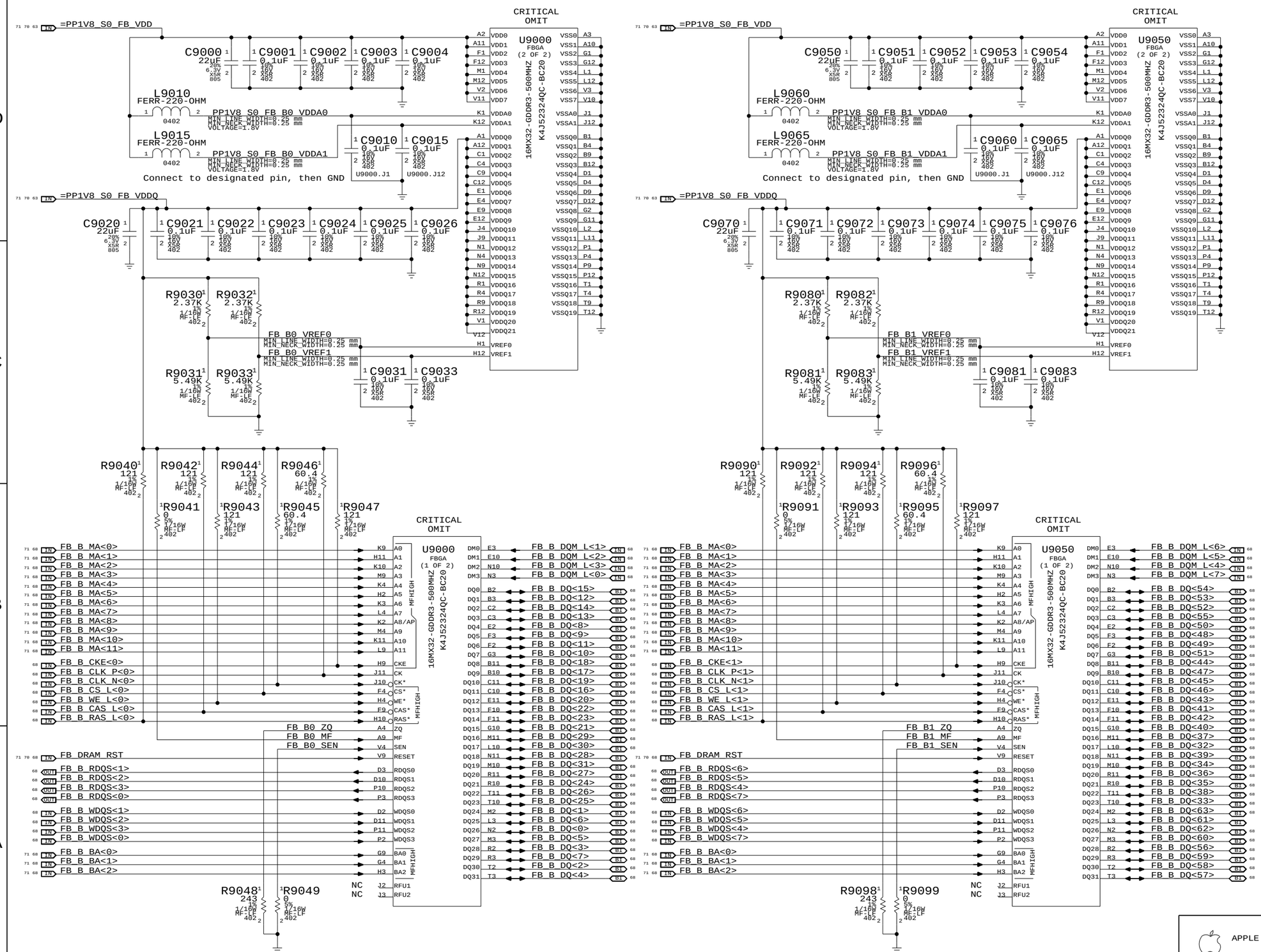
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE NONE	SHT 89 OF 104	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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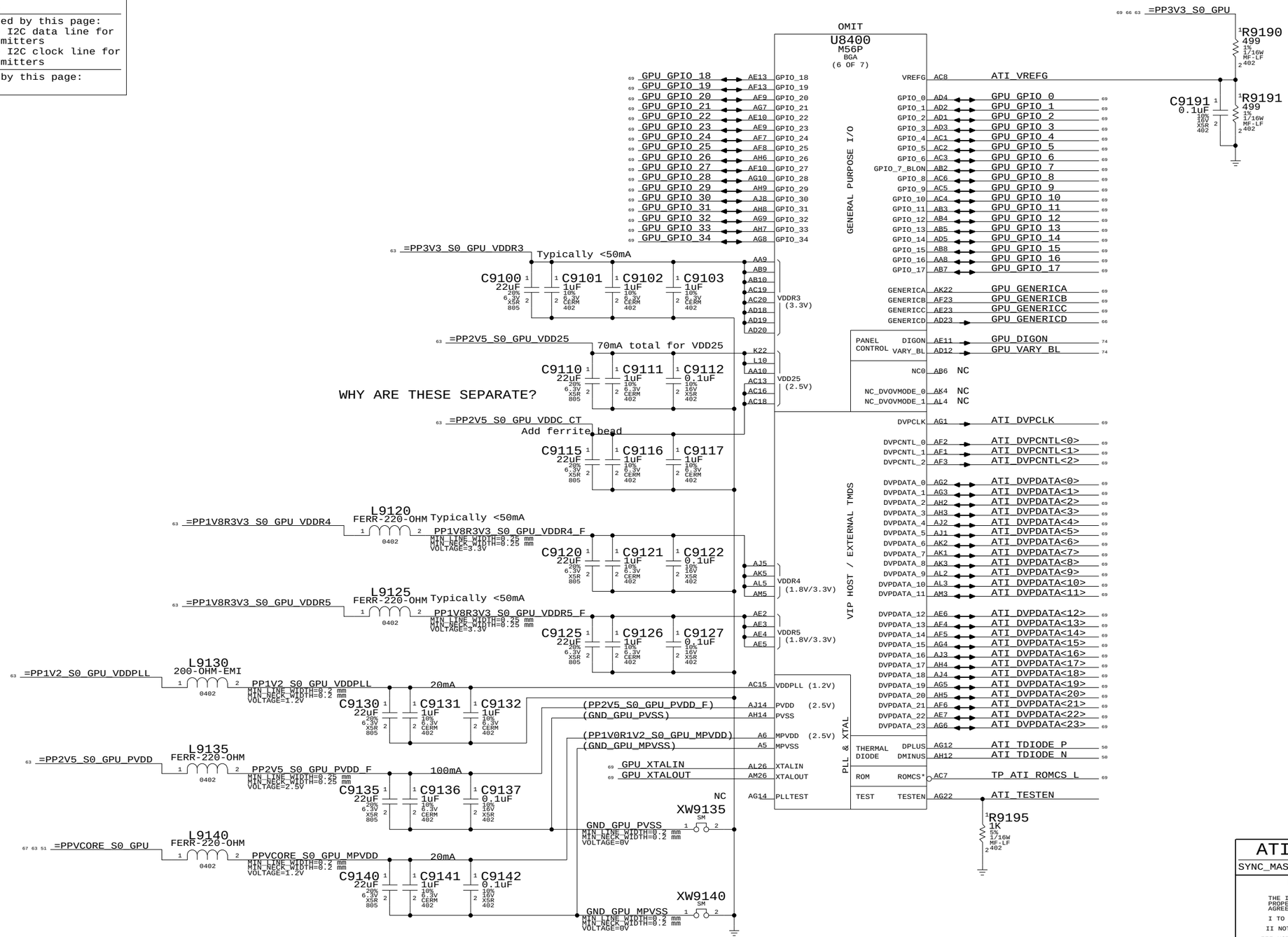
SCALE NONE	SHT 90 OF 104	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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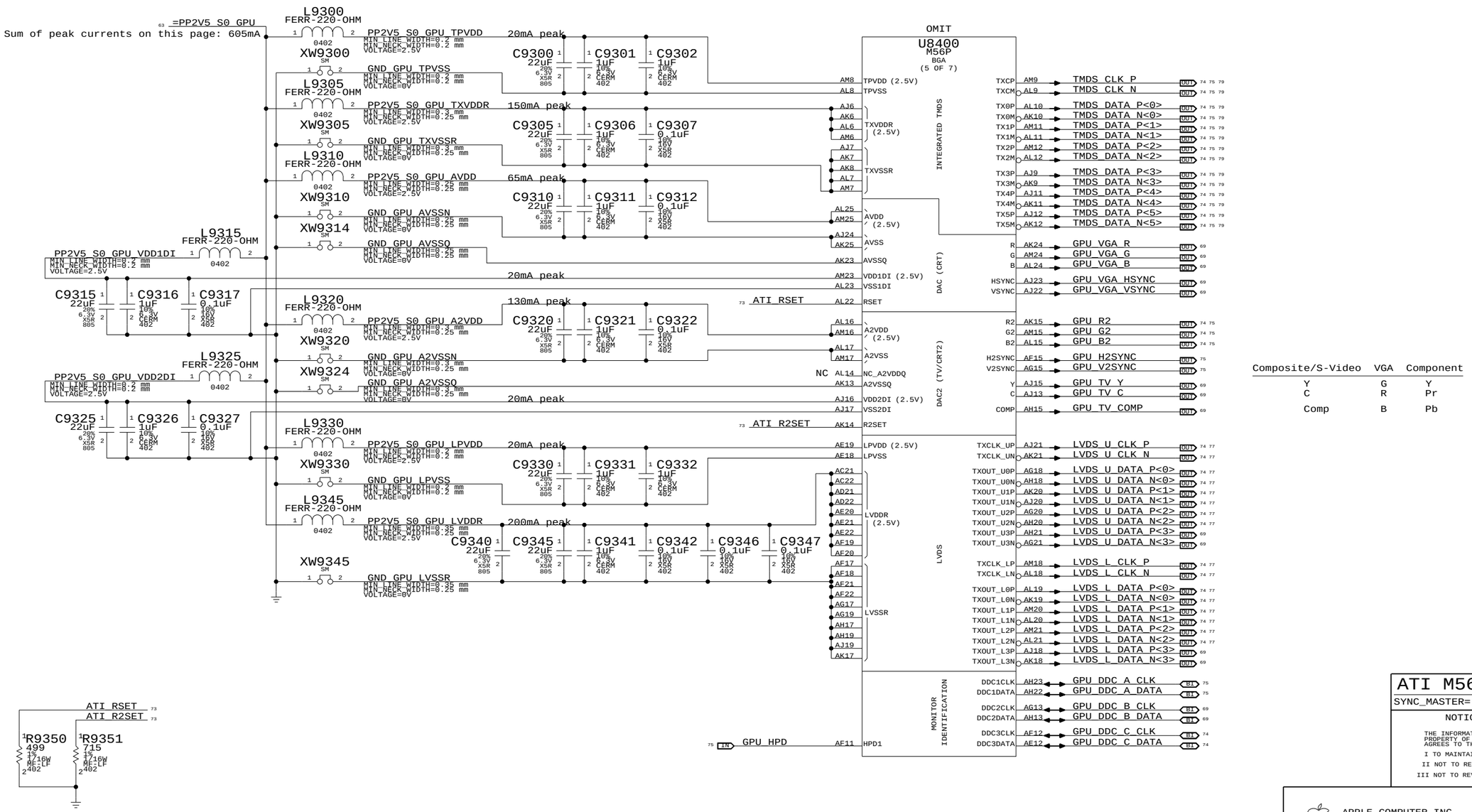
Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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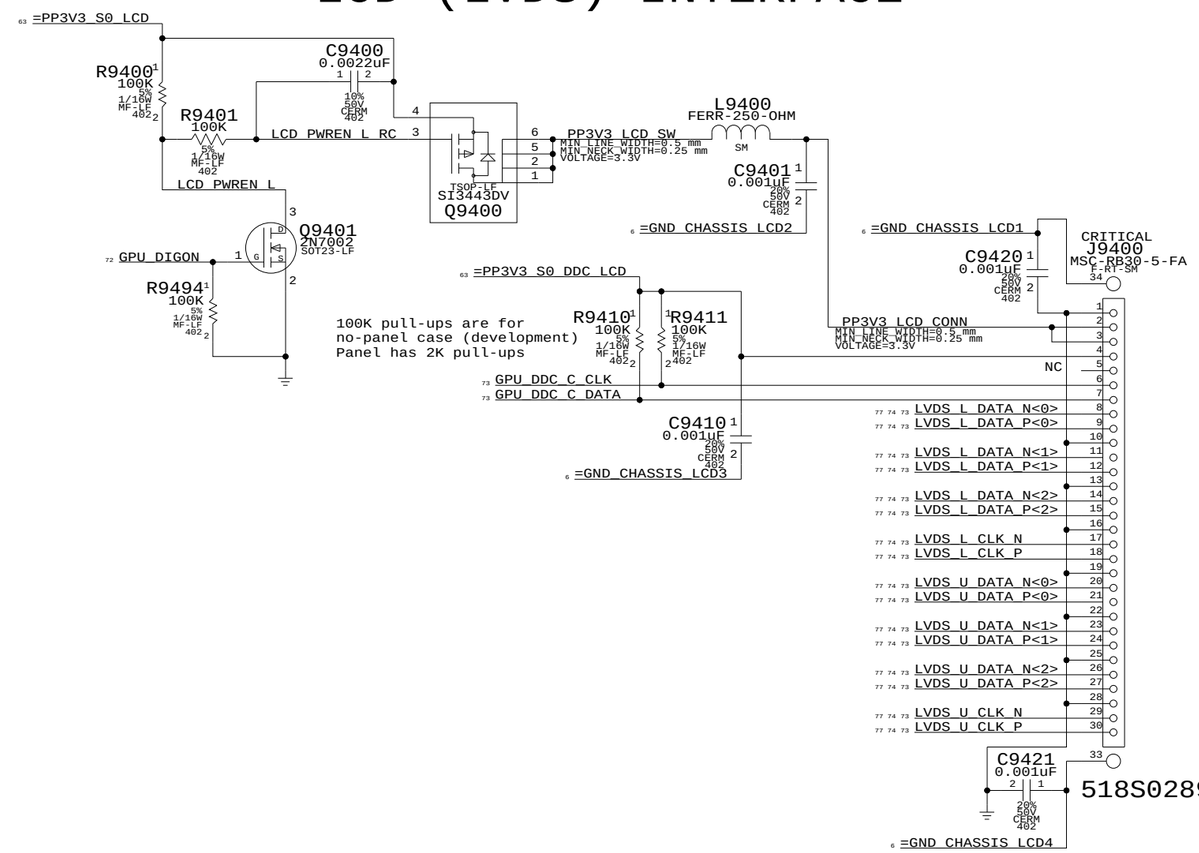
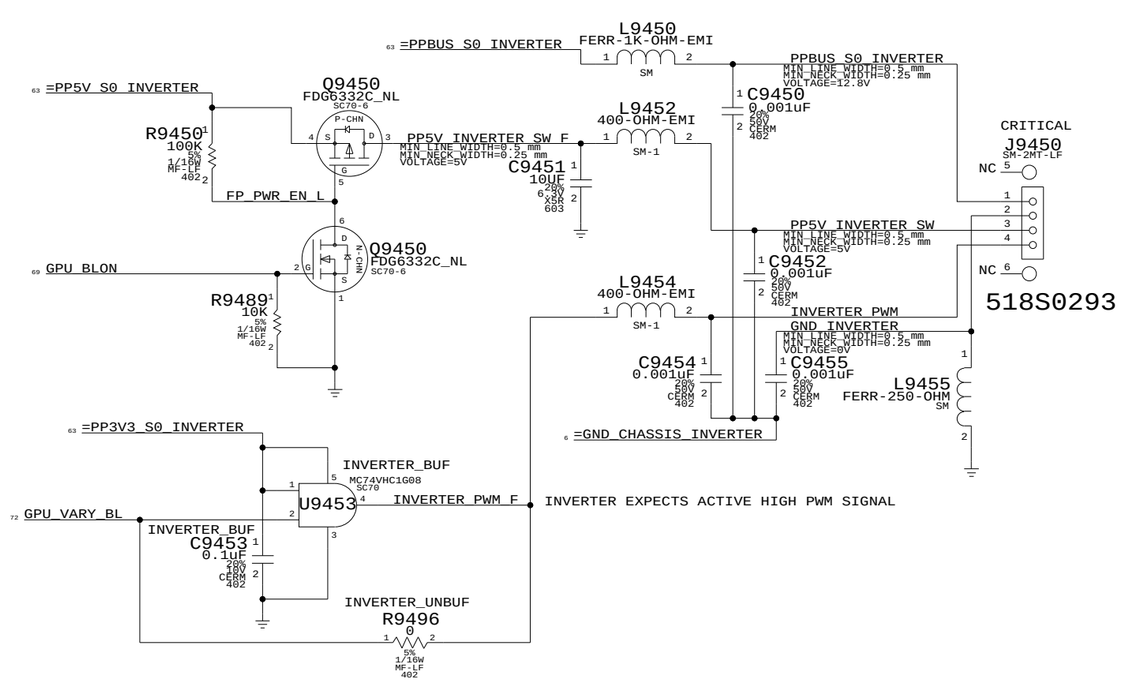
SCALE NONE SHT 93 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 74 77
	LVDS	LVDS	LVDS_U_CLK_N	73 74 77
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 74 77
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 74 77
	LVDS	LVDS	LVDS_L_CLK_P	73 74 77
	LVDS	LVDS	LVDS_L_CLK_N	73 74 77
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 74 77
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 74 77
	TMDS	TMDS	TMDS_CLK_P	73 75 79
	TMDS	TMDS	TMDS_CLK_N	73 75 79
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 79

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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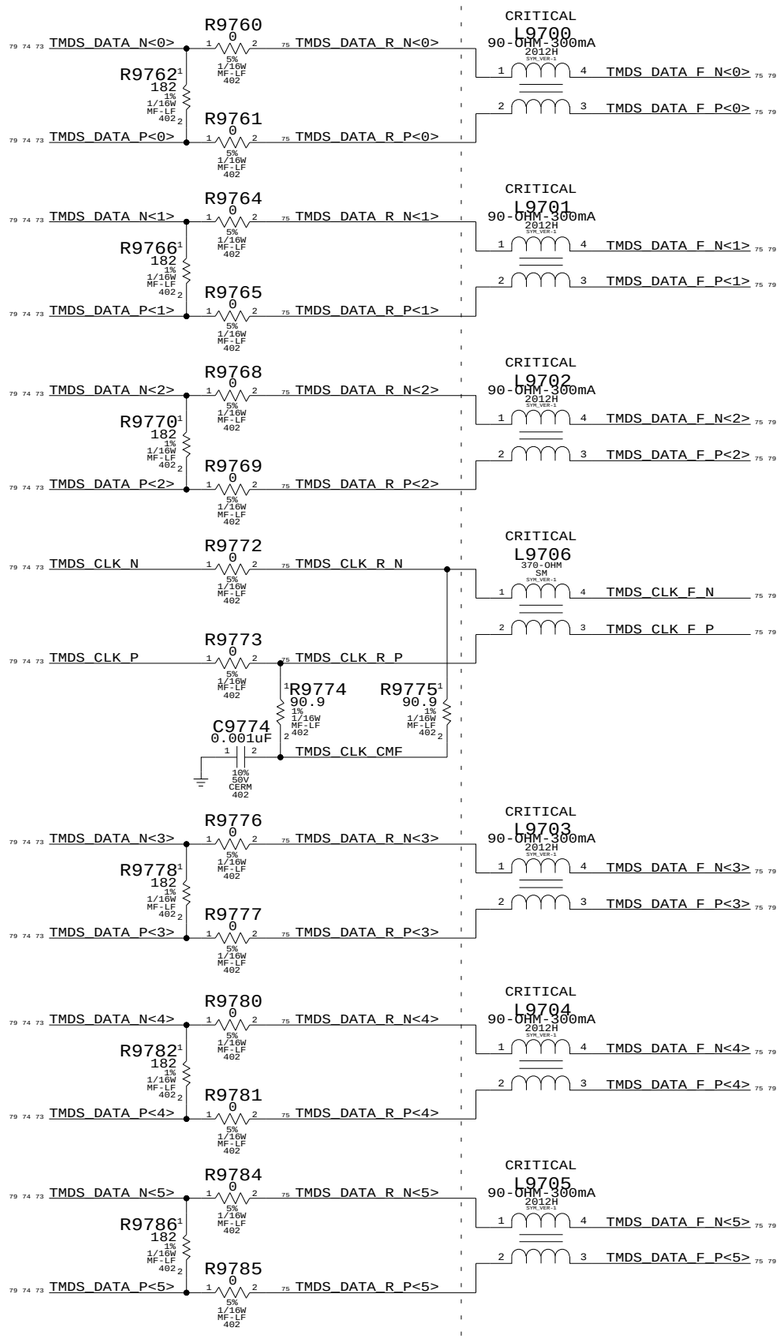
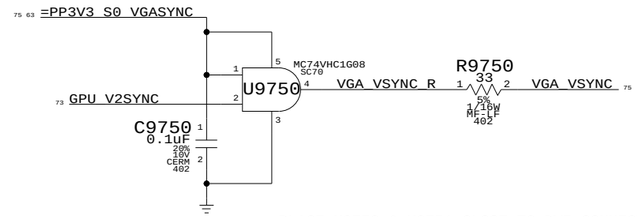
TMDS Filtering

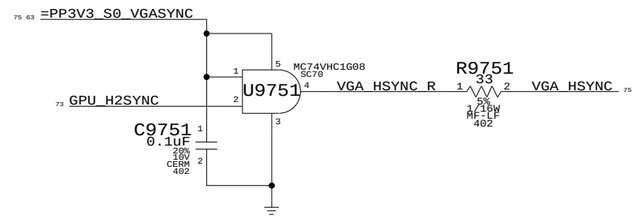
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS

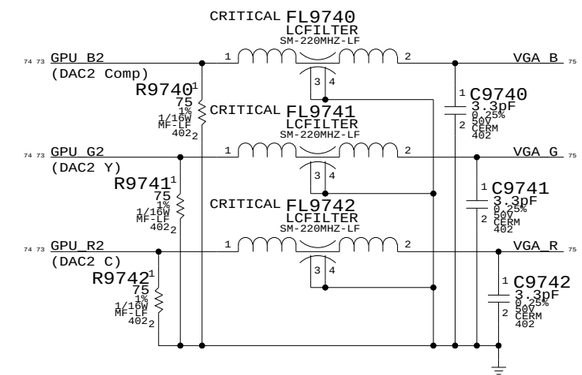


PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR



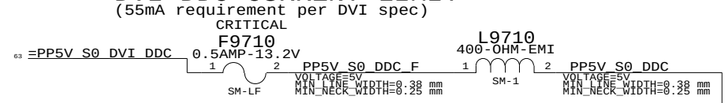
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P
	TMDS	TMDS	TMDS_CLK_R_N
	TMDS	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

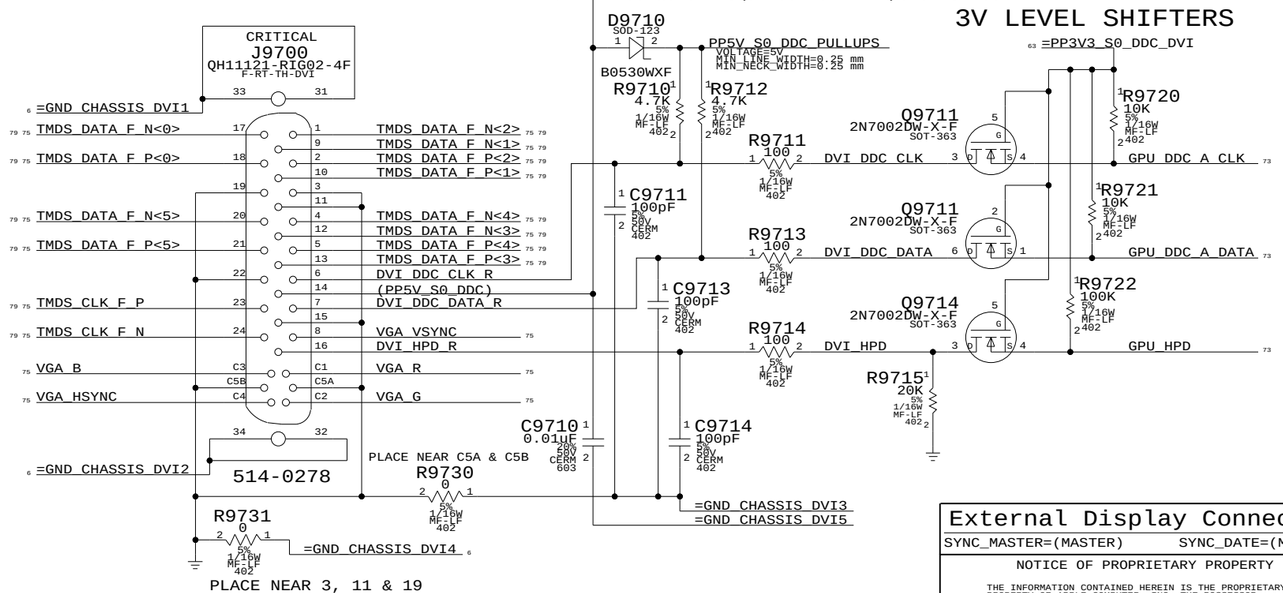


DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



Isolation required for DVI power switch



External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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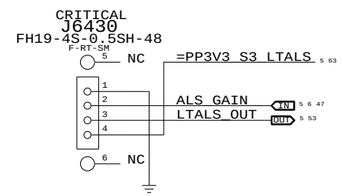
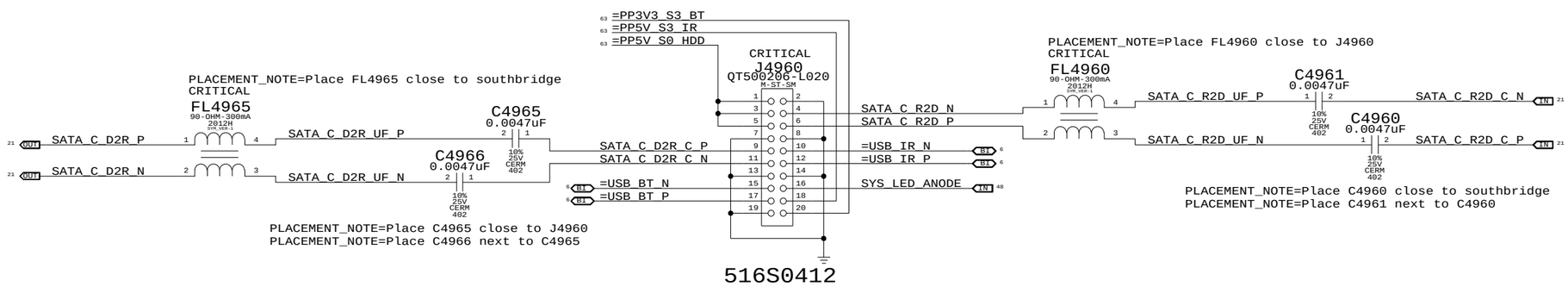
Left ALS Connector



518S0395

Bluetooth (M13P) & SATA HDD Flex Connector



516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M1 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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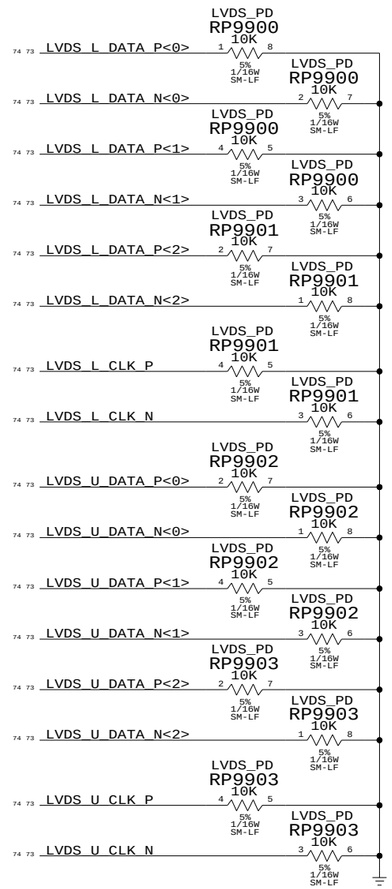
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.

2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42.
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.
2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

Date - Radar # - Description

DMS Checkin #07001

2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.
2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.
(11.5.0) 2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.
2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.
(11.6.0) 2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.
(11.7.0) 2005/09/30 - 4248911 - Sync with M38 & M42.
2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.
2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.

DMS Checkin #07002

2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
(11.8.0) 2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.
2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.
2005/10/06 - 4227330 - Added ESD protection on top-case USB port.
2005/10/07 - 4286888 - BOM restructuring per EVT build plan.
2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.
2005/10/07 - 4248911 - Sync with M38 & M42.

DMS Checkin #07003

(11.9.0) 2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.
2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).
2005/10/08 - 4286729 - Changed value of TPM Xtal caps.
2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.
(11.10.0) 2005/10/09 - 4235898 - Part moves & refdes changes to support sync with M9.
2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.
2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.

DMS Checkin #07004

2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.
2005/10/10 - 4247941 - Net property updates found via back-annotation.

DMS Checkin #07005

2005/10/10 - 4229560 - Removed Physical Security circuitry.
2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.
2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.
2005/10/10 - 4248911 - Sync with M38 & M42.
2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.

DMS Checkin #07006

2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.
2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.
2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.
2005/10/12 - 4248911 - Sync with M38 & M42.
2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.
2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.
2005/10/12 - 4223808 - Power supply changes per vendor feedback.
2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).
2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.
2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.
2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.
2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.
2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.
2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.

DMS Checkin #07007

2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.

DMS Checkin #07008

2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.

DMS Checkin #07009

2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.
2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.
2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.
2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.
2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.

DMS Release #08000-11000 (EVT releases)

2005/10/20 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/10/21 - 4310267 - Synced 3 pages from mlb_evt branch back to trunk.
2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.
2005/10/26 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/11/03 - 4310267 - Synced 6 pages from mlb_evt branch back to trunk.
2005/11/15 - 4310267 - Synced 5 pages from mlb_evt branch back to trunk.
2005/11/15 - 4298899 - Removed unused platform reset gate.
2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.
2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.
2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.
2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.
2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.
2005/11/16 - 4345921 - FUNC_TEST updates per test team request.
2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.
2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.
2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.

DMS Checkin #11001

2005/11/16 - 4235898 - Sync with M38 & M42.
(11.1.0) 2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.
(11.2.0) 2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.
2005/11/18 - 4235898 - Changed R4210 package size per M9 request.
(11.3.0) 2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.
2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.
2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.
2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.
2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.
2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.
2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.
(11.4.0) 2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).

Date - Radar # - Description

DMS Checkin #11002

2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.
2005/11/21 - 4343202 - Changed RC value and net name for USB OC.
2005/11/22 - 4350840 - Swapped TMDS termination components for placement.
2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.
2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.
2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.
2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.
2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.
2005/11/30 - 4351181 - Changed ITP connector BOM option.
2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.
2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.
2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.
2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.
2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.
2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.

DMS Checkin #11003

2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.
2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.
2005/12/02 - 4363870 - Removed M1a support from BOM.
2005/12/02 - 4217524 - Updated part number for J6430.

DMS Release #12000

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SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2T01	CPU_THERMTRIP_L	
	CPU_55S	CPU_2T01	PM_DPRSLPVR	14 23 57
	CPU_55S	CPU_2T01	IMVP_DPRSLPVR	57
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2T01	CPU_VID<6..0>	8 9 79
	CPU_55S	CPU_2T01	CPU_VID<6..0>	8 9 79
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	57

MEM_CLK	MEM_70D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIE	PCIE_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 45
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
AUDIO_55S	AUDIO	ACZ_SYNC	5 21 45
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
AUDIO_55S	AUDIO	ACZ_RST_L	5 21 45
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 45
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 45

TMDS	TMDS	TMDS_CLK_P	73 74 75
TMDS	TMDS	TMDS_CLK_N	73 74 75
TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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